

F DN340P

Single P-Channel, Logic Level, PowerTrench® MOSFET

General Description

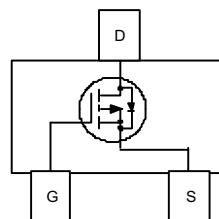
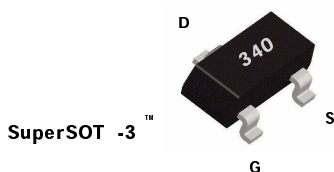
This P-Channel Logic Level MOSFET is produced using Fairchild Semiconductor advanced Power Trench process that has been especially tailored to minimize the on-state resistance and yet maintain low gate charge for superior switching performance.

These devices are well suited for portable electronics applications: load switching and power management, battery charging circuits, and DC/DC conversion.



Features

- -2A, 20 V $R_{DS(ON)} = 70\text{ m}\Omega @ V_{GS} = -4.5\text{ V}$
 $R_{DS(ON)} = 110\text{ m}\Omega @ V_{GS} = -2.5\text{ V}$
- Low gate charge (7.2 nC typical).
- High performance trench technology for extremely low $R_{DS(ON)}$.
- High power version of industry Standard SOT-23 package. Identical pin-out to SOT-23 with 30% higher power handling capability.



Absolute Maximum Ratings $T_A=25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Ratings	Units
V_{DSS}	Drain-Source Voltage	-20	V
V_{GSS}	Gate-Source Voltage	± 8	V
I_b	Drain Current – Continuous (Note 1a)	-2	A
	– Pulsed	-10	
P_D	Power Dissipation for Single Operation (Note 1a) (Note 1b)	0.5	W
		0.46	
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to +150	$^\circ\text{C}$

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1a)	250	$^\circ\text{C/W}$
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case (Note 1)	75	$^\circ\text{C/W}$

Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape width	Quantity
340	F DN340P	7"	8mm	3000 units

Electrical Characteristics

$T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_b = -250\ \mu\text{A}$	-20			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_b = -250\ \mu\text{A}$, Referenced to 25°C		-12		mV/ $^\circ\text{C}$
I_{bSS}	Zero Gate Voltage Drain Current	$V_{DS} = -16\text{ V}, V_{GS} = 0\text{ V}$			-1	μA
		$V_{DS} = -16\text{ V}, V_{GS} = 0\text{ V}, T_J = 55^\circ\text{C}$			-10	
I_{GSSF}	Gate-Body Leakage, Forward	$V_{GS} = 8\text{ V}, V_{DS} = 0\text{ V}$			100	nA
I_{GSSR}	Gate-Body Leakage, Reverse	$V_{GS} = -8\text{ V}, V_{DS} = 0\text{ V}$			-100	nA
On Characteristics (Note 2)						
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_b = -250\ \mu\text{A}$	-0.4	-0.8	-1.5	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	$I_b = -250\ \mu\text{A}$, Referenced to 25°C		3		mV/ $^\circ\text{C}$
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = -4.5\text{ V}, I_b = -2\text{ A}$		60	70	m Ω
		$V_{GS} = -4.5\text{ V}, I_b = -2\text{ A}, T_J = 125^\circ\text{C}$		77	120	
		$V_{GS} = -2.5\text{ V}, I_b = -1.7\text{ A}$		82	110	
$I_{b(on)}$	On-State Drain Current	$V_{GS} = -4.5\text{ V}, V_{DS} = -5\text{ V}$	-5			A
g_{FS}	Forward Transconductance	$V_{DS} = -4.5\text{ V}, I_b = -2\text{ A}$		9		S
Dynamic Characteristics						
600	Input Capacitance	$V_{DS} = -10\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$		779		pF
175	Output Capacitance			121		pF
80	Reverse Transfer Capacitance			56		pF
Switching Characteristics (Note 2)						
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = -10\text{ V}, I_b = -1\text{ A},$ $V_{GS} = -4.5\text{ V}, R_{GEN} = 6\ \Omega$		10	20	ns
t_r	Turn-On Rise Time			9	10	ns
$t_{d(off)}$	Turn-Off Delay Time			27	43	ns
t_f	Turn-Off Fall Time			11	20	ns
Q_g	Total Gate Charge	$V_{DS} = -10\text{ V}, I_b = -3.5\text{ A},$ $V_{GS} = -4.5\text{ V}$		7.2	10	nC
Q_{gs}	Gate-Source Charge			1.7		nC
Q_{gd}	Gate-Drain Charge			1.5		nC
Drain-Source Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Drain-Source Diode Forward Current				-0.42	A
V_{SD}	Drain-Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = -0.42\text{ A}$ (Note 2)		-0.7	-1.2	V

Notes:

- $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a. 250°C/W when mounted on a 0.02 in^2 pad of 2 oz copper



b. 270°C/W when mounted on a $.001\text{ in}^2$ pad of 2 oz copper

Scale 1 : 1 on letter size paper

- Pulse Test: Pulse Width < $300\ \mu\text{s}$, Duty Cycle < 2.0%

Typical Characteristics

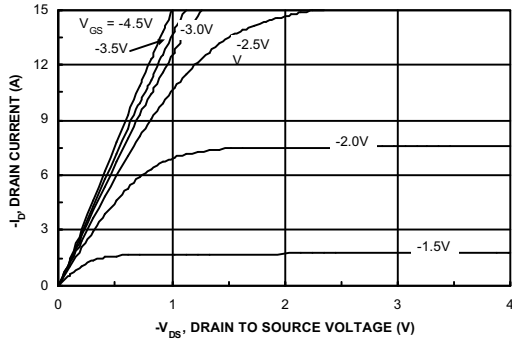


Figure 1. On-Region Characteristics.

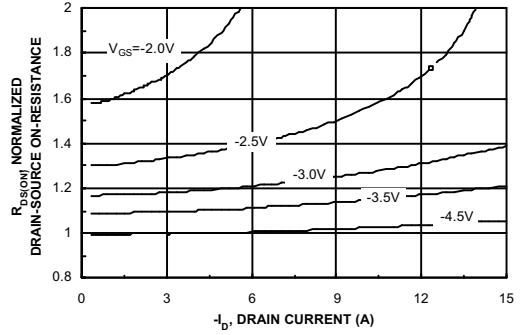


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

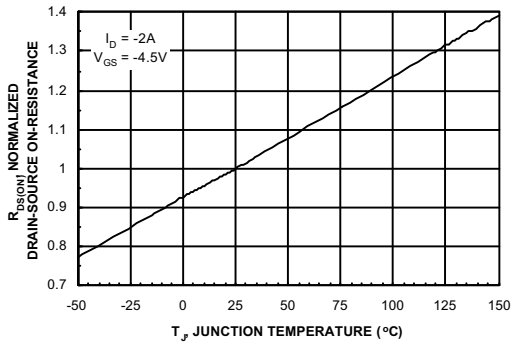


Figure 3. On-Resistance Variation with Temperature.

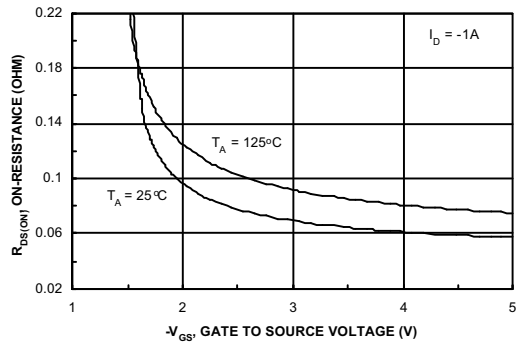


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

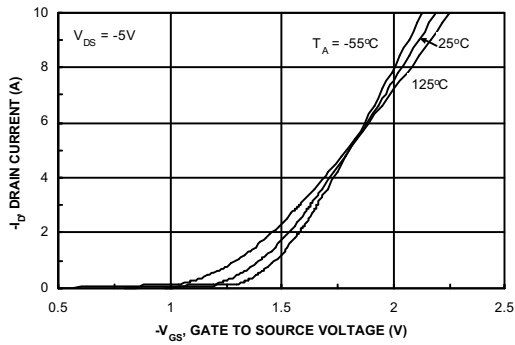


Figure 5. Transfer Characteristics.

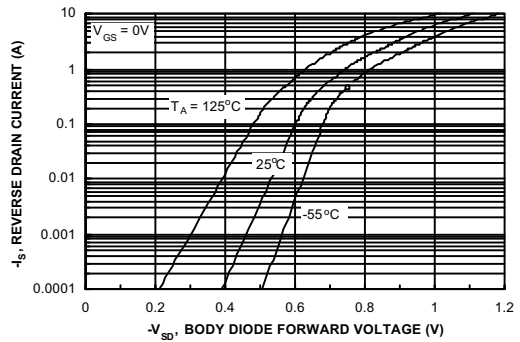


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Characteristics

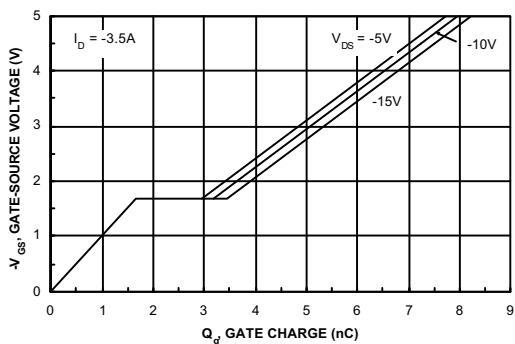


Figure 7. Gate Charge Characteristics.

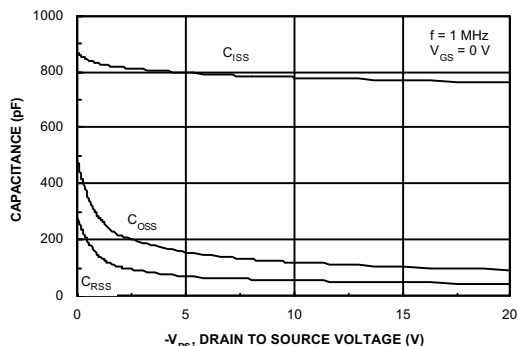


Figure 8. Capacitance Characteristics.

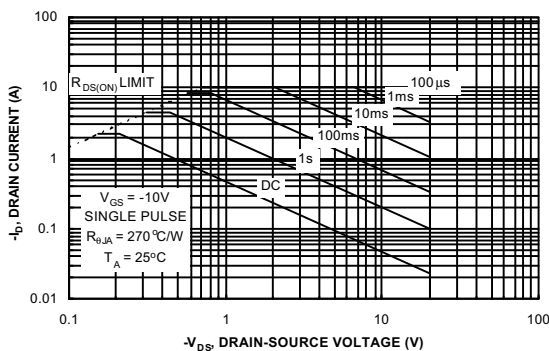


Figure 9. Maximum Safe Operating Area.

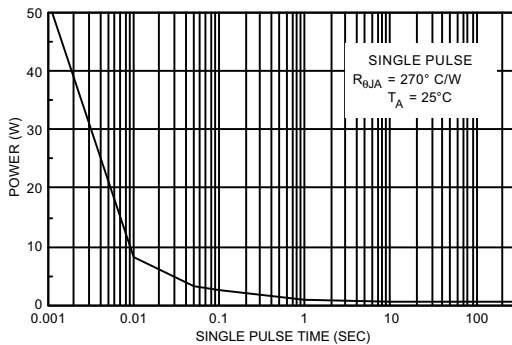


Figure 10. Single Pulse Maximum Power Dissipation.

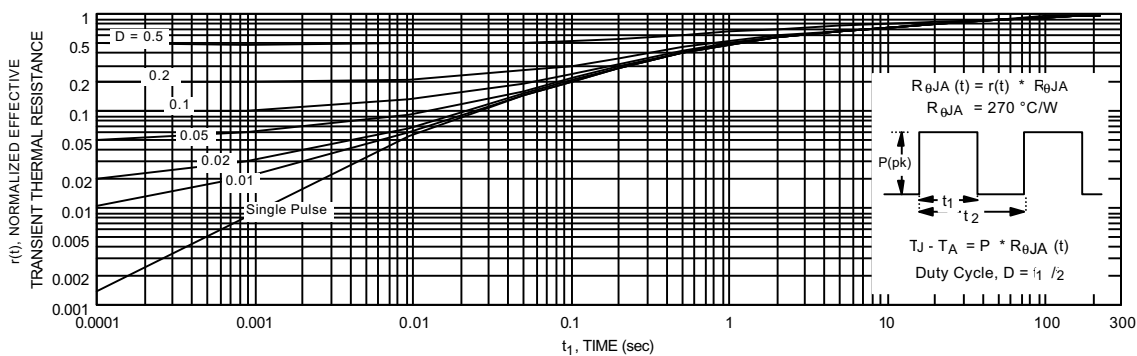


Figure 11. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1b. Transient thermal response will change depending on the circuit board design.

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