National Semiconductor

GAL22V10, -15, -20, -25, -30 Generic Array Logic

General Description

The NSC E²CMOS™ GAL® devices combine a high performance CMOS process with electrically erasable floating gate technology. This programmable memory technology applied to array logic provides designers with reconfigurable logic and bipolar performance at significantly reduced power levels.

The 24-pin GAL22V10 features 22 inputs, and 10 programmable Output Logic Macro Cells (OLMCs) allowing each TRI-STATE® output to be configured by the user. The architecture of each output is user-programmable for registered or combinatorial operation, active high or low polarity, and as an input, output or bidirectional I/O. This architecture features variable product term distribution, from 8 to 16 logical product terms to each output, as shown in the logic diagram. CMOS circuitry allows the GAL22V10 to consume just 90 mA typical I_{CC} which represents a 50% saving in power when compared to its bipolar counterparts. Synchronous preset and asynchronous reset product terms have been added which are common to all output registers to enhance system operation. The GAL22V10 is directly compatible with the bipolar PAL22V10 in terms of functionality, fuse map, pinout, and electrical characteristics.

Programming is accomplished using industry standard available hardware and software tools. NSC guarantees a minimum 100 erase/write cycles.

Unique test circuitry and reprogrammable cells allow complete AC, DC, cell and functionality testing during manufacture. Therefore, NSC guarantees 100% field programmability of all GAL devices. In addition, electronic signature is available to provide positive device ID. A security circuit is built-in, providing proprietary designs with copy protection.

Features

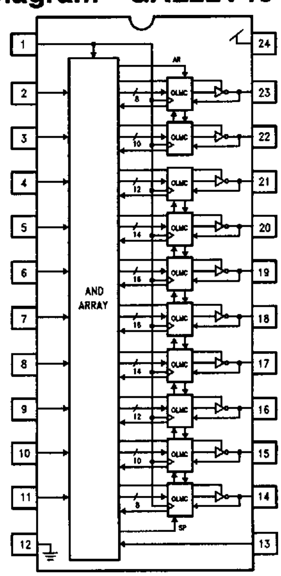
- High performance E²CMOS technology
  - 15 ns maximum propagation delay
  - f_{max} = 45 MHz with feedback
  - TTL compatible 16 mA outputs
  - UltraMOS® III advanced CMOS technology
  - Internal pull-up resistor on all pins
- Electrically erasable cell technology
  - Reconfigurable logic
  - Reprogrammable cells
  - 100% tested/guaranteed 100% yields
  - High speed electrical erasure (<50 ms)
  - 20 year data retention
- Ten output logic macrocells
  - Maximum Flexibility
  - Programmable output polarity
  - Maximum flexibility for complex logic designs
  - Full function/fuse map/parametric compatibility with PAL22V10 devices
- Variable product term distribution
  - From 8 to 16 product terms per output data function
- Global synchronous preset and asynchronous reset
- Preload and power-up reset of all registers
  - 100% functional testability
- Fully supported by National OPAL™ and OPALjr development software
- Security cell prevents copying logic

Ordering Information

GAL 22 V 10 - 15 L N C

- GAL — Generic Array Logic Family
- 22 — Number of Array Inputs
- V — Output Type: V = Variable Architecture
- 10 — Number of Outputs
- 15 — Speed:
  - 15: t_{PD} = 15 ns (Com)
  - 20: t_{PD} = 20 ns (Ind)
  - 25: t_{PD} = 25 ns (Com)
  - 30: t_{PD} = 30 ns (Ind)
- L = Low Power
- N — Package Type:
  - N = 24-Pin Plastic DIP
  - V = 28-Lead Plastic Chip Carrier
- C — Temperature Range:
  - C = Commercial (0°C to +75°C)
  - I = Industrial (−40°C to +85°C)

Block Diagram—GAL22V10



TL/L/10406-2

Absolute Maximum Ratings (Note 1)

Supply Voltage (V_{CC}) (Note 2) −0.5V to +7.0V

Input Voltage (Note 2) −2.5V to V_{CC} +1.0V

Off-State Output Voltage (Note 2) −2.5V to V_{CC} +1.0V

Output Current ±100 mA

Storage Temperature −65°C to +150°C

Ambient Temperature with Power Applied −65°C to +125°C

Junction Temperature −65°C to +150°C

Lead Temperature (Soldering, 10 seconds) 260°C

ESD Tolerance 700V
C_{ZAP} = 100 pF
R_{ZAP} = 1500Ω

Test Method: Human Body Model

Test Specification: NSC SOP-5-028

Recommended Operating Conditions

SUPPLY VOLTAGE AND TEMPERATURE

Symbol	Parameter	Commercial			Industrial			Units
		Min	Typ	Max	Min	Typ	Max	
V_{CC}	Supply Voltage	4.75	5	5.25	4.5	5	5.5	V
T_A	Operating Free-Air Temperature	0	25	75	−40	25	85	°C

AC TIMING REQUIREMENTS

Symbol	Parameter		GAL22V10-15L		GAL22V10-20L		GAL22V10-25L		GAL22V10-30L		Units
			COM		IND		COM		IND		
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{SU}	Set-Up Time (Input or Feedback before Clock)		12		15		15		25		ns
t_H	Hold Time (Input after Clock)		0		0		0		0		ns
t_W	Clock Pulse Width (High/Low)		8		10		15		20		ns
t_{AW}	Asynchronous Reset Input Pulse Width		15		20		25		30		ns
t_{AR}	Asynchronous Reset Recovery Time		15		20		25		30		ns
t_{CYCLE}	Clock Cycle Period (with Feedback) (Note 3)		22		27		30		45		ns
f_{CLK}	Clock Frequency (Note 4)	With Feedback		45.5		34.5		33.3		22.2	MHz
		Without Feedback		62.5		50		33.3		25	MHz
f_I	Input Frequency (Note 5)			66.6		50.0		40.0		33.3	MHz
t_{PR}	Clock Valid after Power-Up			100		100		100		100	ns

Note 1: Absolute maximum ratings are those values beyond which the device may be permanently damaged. Proper operation is not guaranteed outside the specified recommended operating conditions.

Note 2: Some device pins may be raised above these limits during programming and preload operations according to the applicable specification.

Note 3: $t_{CYCLE} = t_{SU} + t_{CLK}$

Note 4: f_{CLK} (with feedback) = $(t_{CYCLE})^{-1}$
f_{CLK} (without feedback) = $(2\ t_w)^{-1}$

Note 5: $f_I = (t_{PD})^{-1}$

Electrical Characteristics Over Recommended Operating Conditions

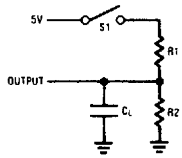
Symbol	Parameter	Conditions		Temperature Range	Min	Typ	Max	Units
V_{IH}	High Level Input Voltage				2.0		$V_{CC}+1$	V
V_{IL}	Low Level Input Voltage				$V_{SS}-0.5$		0.8	V
V_{OH}	High Level Output Voltage	V_{CC} = Min	I_{OH} = −3.2 mA	COM/IND	2.4			V
V_{OL}	Low Level Output Voltage	V_{CC} = Min	I_{OL} = 16 mA	COM/IND			0.5	V
I_{OZH}	High Level Off State Output Current	V_{CC} = Max, V_O = V_{CC} (Max)					10	µA
I_{OZL}	Low Level Off State Output Current	V_{CC} = Max, V_O = GND					−150	µA
I_I	Maximum Input Current	V_{CC} = Max, V_I = V_{CC} (Max)			−150		10	µA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = V_{CC} (Max)					10	µA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = GND					−150	µA
I_{OS}*	Output Short Circuit Current	V_{CC} = 5.0V, V_O = GND			−30		−150	mA
I_{CC}	Supply Current	f = 25 MHz, V_{CC} = Max		COM		90	130	mA
				IND			150	mA
C_I	Input Capacitance	V_{CC} = 5.0V, V_I = 2.0V					8	pF
$C_{I/O}$	I/O Capacitance	V_{CC} = 5.0V, $V_{I/O}$ = 2.0V					10	pF

*One output at a time for a maximum duration of one second.

Switching Characteristics Over Recommended Operating Conditions

Symbol	Parameter	Conditions	GAL22V10-15L		GAL22V10-20L		GAL22V10-25L		GAL22V10-30L		Units
			COM		IND		COM		IND		
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{PD}	Input or Feedback to Combinatorial Output	S1 Closed, C_L = 50 pF		15		20		25		30	ns
t_{CLK}	Clock to Registered Output or Feedback	S1 Closed, C_L = 50 pF		10		12		15		20	ns
t_{PZXI}	Input to Combinatorial Output Enabled via Product Term	Active High; S1 Open, C_L = 50 pF Active Low; S1 Closed, C_L = 50 pF		15		20		25		25	ns
t_{PXZI}	Input to Combinatorial Output Disabled via Product Term	From V_{OH}; S1 Open, C_L = 5 pF From V_{OL}; S1 Closed, C_L = 5 pF		15		20		25		25	ns
t_{AP}	Asynchronous Reset Input to Register Output			20		25		25		30	ns
t_{RESET}	Power-Up to Registered Output High	S1 Closed, C_L = 50 pF		45		45		45		45	µs

AC Test Load

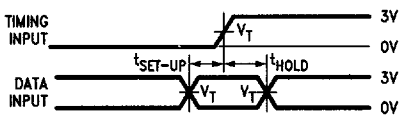


COM'L/IND
R1 = 300
R2 = 390

TL/L/10406-3

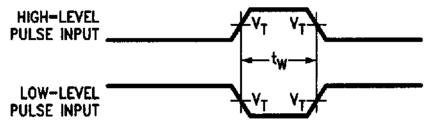
Test Waveforms

Setup and Hold



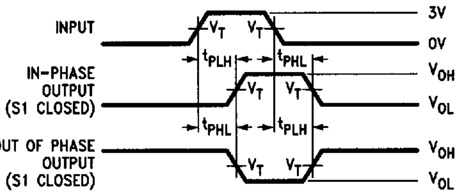
TL/L/10406-4

Pulse Width



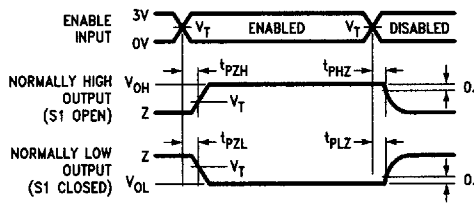
TL/L/10406-5

Propagation Delay



TL/L/10406-6

Enable and Disable



TL/L/10406-7

Notes:

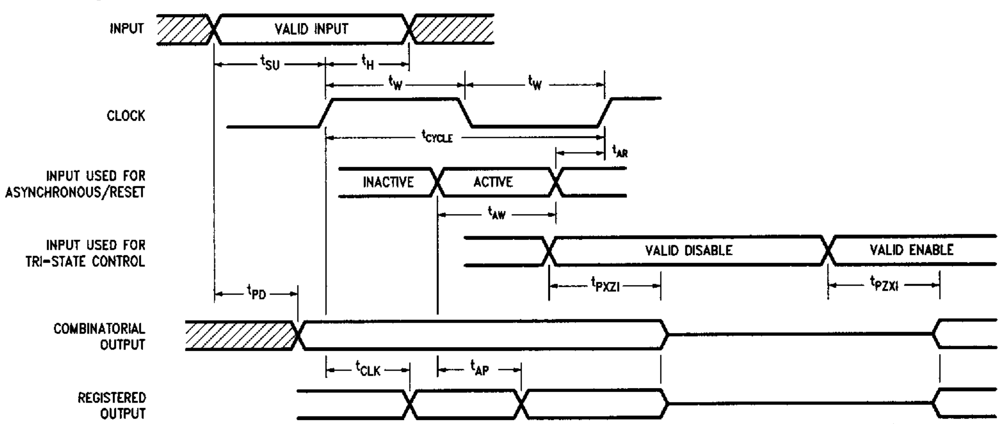
C_L includes probe and jig capacitance.

V_T = 1.5V.

Test inputs have rise and fall times of 3 ns 10%–90%.

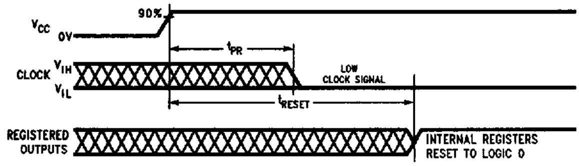
In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.

Switching Waveforms



TL/L/10406-8

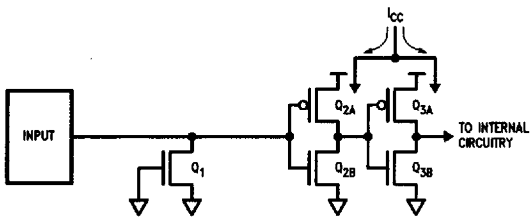
Power-Up Reset Waveforms



TL/L/10406-9

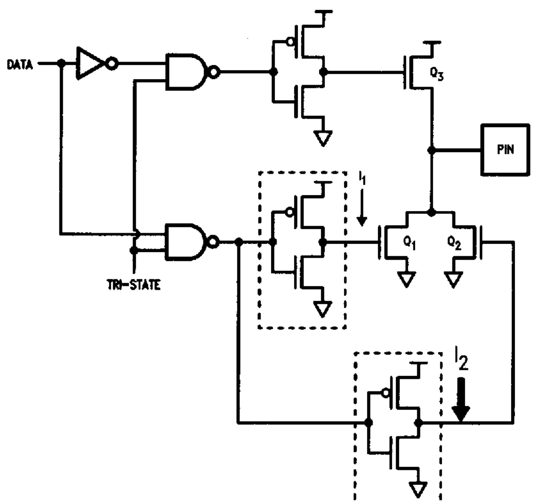
Input/Output Schematics

Input Translator/Buffer



TL/L/10406-22

Phased Output Turn-On Circuit



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Functional Description

The GAL22V10 logic array consists of a programmable AND array with fixed OR-gate connections, similar to the traditional bipolar PAL architecture. The logic array is organized as 22 complementary input lines crossing 132 "product term" lines with a programmable E^2PROM cell at each intersection (5808 cells). Each programmable cell may establish a connection between an input line (true or complement phase of an array input signal) and a product term. A product term is satisfied (logically true) while all of the input lines "connected" to it are in the high logic state.

Of the 132 product terms, 130 are distributed among ten "output logic macrocells" (OLMCs) with a varying number of terms allocated to each OLMC (as shown in *Figure 1*). The ten OLMCs control the flow of input and output signals between the logic array and the device's I/O pins. For a given OLMC, 8, 10, 12, 14 or 16 product terms feed into an OR-gate to produce each output value. This varied distribution of product terms among outputs allows more optimum use of device resources. One additional product term in each of the ten OLMCs is used to control the associated TRI-STATE device output. One global product term is used to control an asynchronous preset, and another global product term is used for a synchronous reset, and both are connected to all ten of the output registers.

The fundamental transfer function of each GAL22V10 output is the familiar Boolean sum-of-products. Design development software is available which accepts Boolean equations and converts them automatically into GAL22V10 programming patterns.

Under control of an OLMC, each output may be designated either registered or combinatorial (non-registered). In the registered output configuration, the logic function output passes through a D-type flip-flop triggered by the rising edge of the clock input. Additionally, the logic function's output polarity may be designated active-low or active-high (adjusted after the register, if present). OLMC options such as these are selected using a set of programmable architecture control cells. These architecture cells are normally configured automatically by the development software or programming hardware.

The four possible I/O configurations of each GAL22V10 OLMC are: registered-active low, registered-active high, combinatorial-active low, and combinatorial-active high. These combinations are shown in *Figure 3*. The feedback paths are redirected with the register selection. The registered configurations include an internal feedback path taken directly from the register output. The combinatorial configurations include feedback from the I/O pin, thus allowing for bidirectional I/O or additional input channels.

All registers in a GAL22V10 device are reset to the low state upon power-up. Outputs, in turn, assume either low or high logic levels (if enabled) depending on the selected output polarity. Power-up reset may simplify sequential circuit design and test. To ensure successful power-up reset, V_{CC} must rise monotonically until the specified operating voltage is attained. During power-up, the clock input should be low as early as possible (within the specified time, t_{PR}) to avoid interfering with the reset operation. The clock input should also remain stable until after the power-up reset operation is completed to allow the registers to capture the proper next state on the first high-going clock transition.

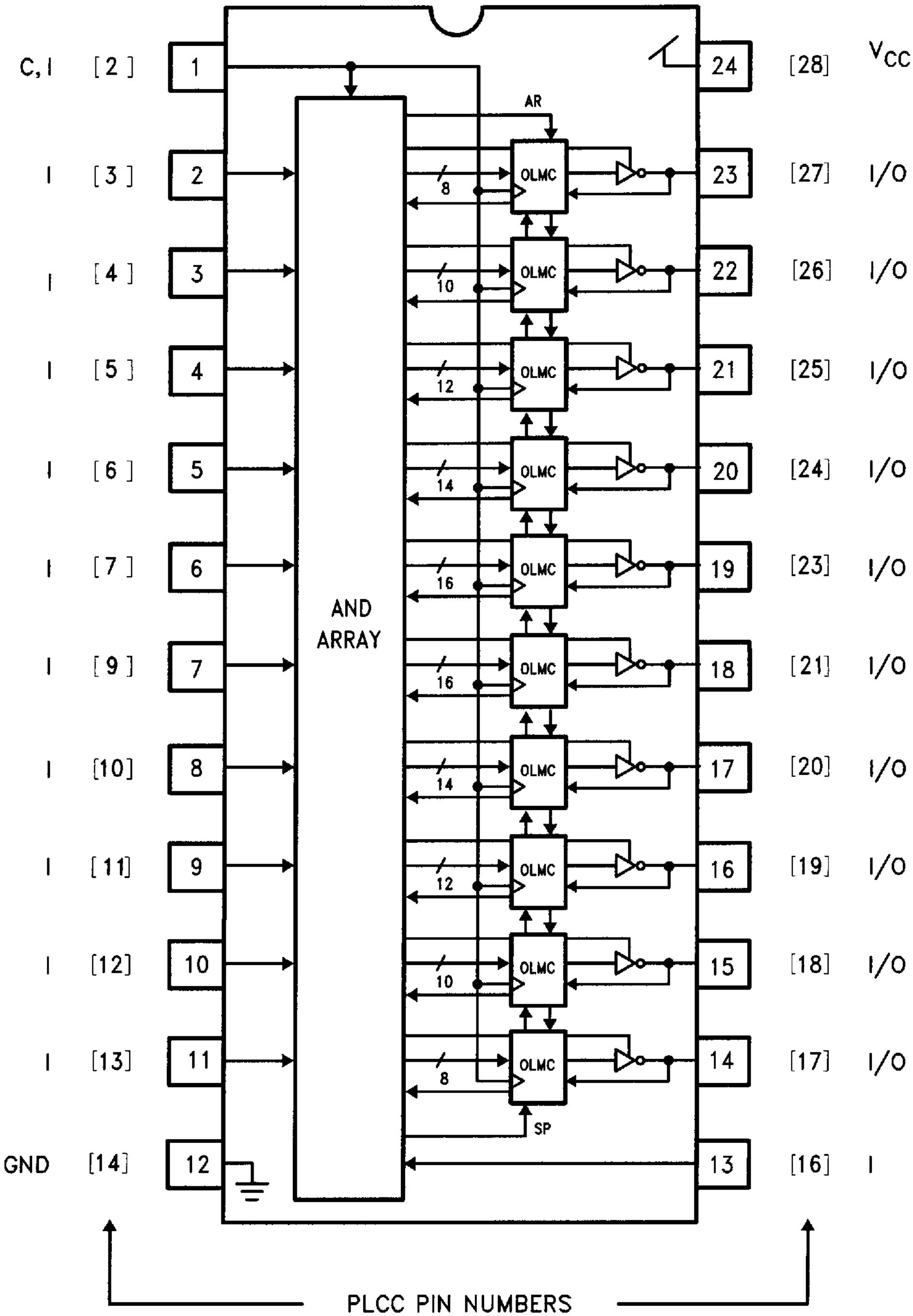
It should be noted that the switching of any input not logically connected to a product term or logic function has no effect on the associated output logic state.

Programmable Preset and Reset

The ten macrocell flip-flops share common programmable preset and reset control for easy system initialization. The Q outputs of the register will go to the logic high state following a low-to-high transition of the clock input when the synchronous preset (SP) product term is asserted. The register will be forced to the logic low state independent of the clock when the asynchronous reset (AR) product term is asserted. Product term control allows preset and reset to be functions of any combination of device inputs and output feedback. The outputs will be high or low depending upon the polarity option chosen.

Note that preset and reset control the flip-flop, not the output. Thus, if active low polarity is selected, a synchronous preset would produce low-level outputs, and an asynchronous reset would produce high-level outputs (if enabled).

GAL22V10 Block Diagram—DIP Connections



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PCC Pin Numbers
FIGURE 1

28-Lead PLCC Connection Diagram

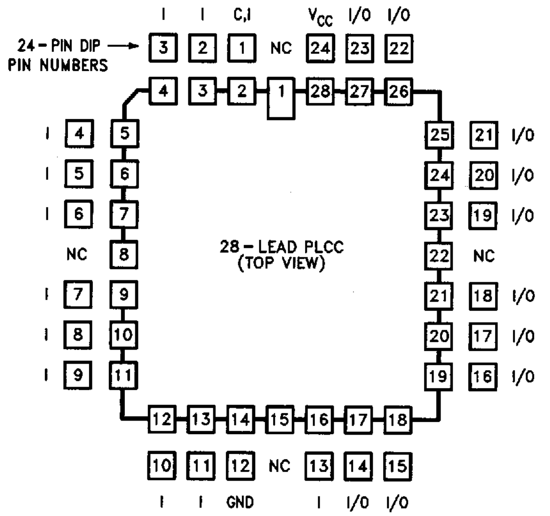

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FIGURE 2

Clock/Input Frequency Specifications

The clock frequency (f_{CLK}) parameter listed in the Recommended Operating Conditions table specifies the maximum speed at which the GAL22V10 registers are guaranteed to operate. Clock frequency is defined differently for the two cases in which register feedback is used versus when it is not. In a data-path type application, when the logic functions fed into the registers are not dependent on register feedback from the previous cycle (i.e. based only on external inputs), the minimum required cycle period (f_{CLK}^{-1} without feedback) is defined as the greater of the minimum clock period (t_w high + t_w low) and the minimum "data window" period (t_{SU} + t_H). This assumes optimal alignment between data inputs and the clock input. In sequential logic applications such as state machines, the minimum required cycle period ($t_{CYCLE} = f_{CLK}^{-1}$ with feedback) is defined as t_{CLK} + t_{SU}. This provides sufficient time for outputs from the registers to feed back through the logic array and set up on the inputs to the registers before the end of each cycle.

The input frequency (f_I) parameter specifies the maximum rate at which each GAL22V10 input can be toggled and still produce valid logic transitions on each combinatorial output. The f_I specification is derived as the inverse of the combinatorial propagation delay (t_{PD}).

Design Development Support

A variety of software tools and programming equipment are available to support the development of designs using GAL22V10 products. Typical software packages, including National's OPAL software, accept Boolean logic equations to define desired functions. Most are available to run on personal computers and generate a JEDEC-compatible "cell-map" (analogous to a PAL "fuse-map"). The industry-standard JEDEC format ensures that the resulting cell-map file can be down-loaded into industry standard programming equipment. Many software packages and programming units support a multitude of programmable logic products as well. The OPAL software package from National Semiconductor supports all programmable logic products available from National and is fully JEDEC-compatible. OPAL software also provides automatic device selection based on the designer's Boolean logic equations.

National strongly recommends using only approved programming hardware and software for developing GAL designs. Programming using unapproved equipment generally voids all guarantees. Approved programmers incorporate specialized programming algorithms that program the array and automatically configure the architecture cells. To ensure data retention and reliability, the programming algorithm also tracks the number of programming cycles to which each GAL device has been subjected since shipment, and stores this information automatically in the device.

The GAL22V10 can accept fuse-maps prepared for other PAL22V10 devices. PAL22V10 fuse-maps can be created by any JEDEC-compatible PAL development software or by loading the fuse pattern from an existing programmed PAL22V10 device into the programming unit (provided the PAL device has not been secured).

Detailed logic diagrams showing all JEDEC cell-map addresses in the GAL22V10 logic array and OLMC are provided for direct map editing and diagnostic purposes. *Figure 6* and Table II show details of the OLMC and the programmable architecture cell combinations. *Figure 7* shows the JEDEC logic diagram and details of all programmable cell locations. For a list of current software and programming support tools available for these devices, please contact your local National sales representative or distributor. If detailed specifications of the GAL22V10 programming algorithm are needed, please contact the National Semiconductor Programmable Device Support department.

OLMC Selection Table

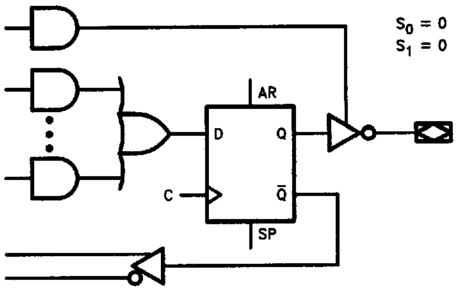

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FIGURE 3-1. Registered/Active Low

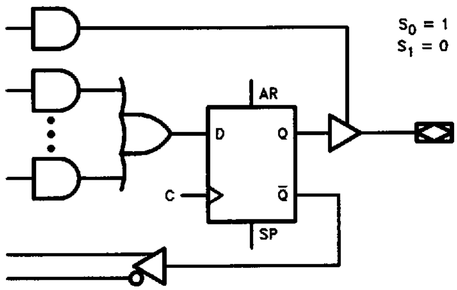

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FIGURE 3-2. Registered/Active High

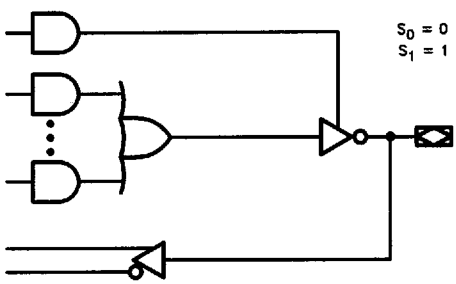

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FIGURE 3-3. Combinatorial/Active Low

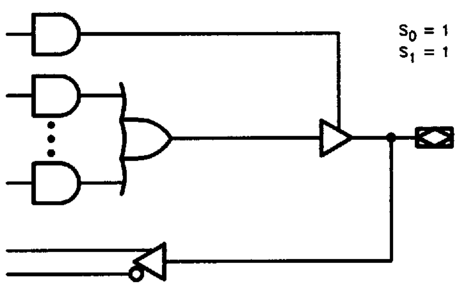

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FIGURE 3-4. Combinatorial/Active High

Security Cell

A security cell is provided on all GAL22V10 devices as a deterrent to unauthorized copying of the array configuration patterns. Once programmed, the circuitry enabling array access is disabled, preventing further programming or verification of the array. The security cell can be erased only in conjunction with the array during a bulk erase cycle, so the original configuration can never be examined once this cell is programmed.

Electronic Signature

Each GAL device contains an electronic signature word consisting of 64 bits of reprogrammable memory. The electronic signature word can be programmed to contain any identification information desired by the user. Some uses include pattern identification labels, revision numbers, dates, inventory control information, etc. The data stored in the electronic signature word has no effect on the functionality of the device. The information is read out of the device using the normal program verification procedure provided by the programming equipment. The information may be accessed at any time independent of the state of the security cell. National's OPAL development software allows electronic signature data to be entered by the user and downloaded to the programming equipment.

Bulk Erase

The programming equipment automatically performs a bulk erase operation prior to each programming operation. No special erase operation need be performed by the user. Bulk erase clears the logic array, architecture cells, security cell, and electronic signature information. The GAL device is thereby reverted back to its virgin state.

Latch-Up Protection

GAL devices are designed with an on-chip charge pump to negatively bias the substrate. The negative bias is of sufficient magnitude to prevent input undershoots from causing the circuitry to latch. Additionally, outputs are designed with n-channel pullups instead of the traditional p-channel pullups to eliminate any possibility of SCR induced latching.

Manufacturer Testing

Because of E^2CMOS technology, GAL devices can be reprogrammed in milliseconds. This allows each device to be completely tested by the manufacturer using numerous logic array and architecture patterns prior to shipping. Every programmable cell and every logic path through every device is fully tested for programmability, functionality and performance to all AC and DC parameters. The customer can therefore expect 100% programming and functional yield and 100% compliance of all GAL products to datasheet specifications.

The testing procedure performed on all GAL devices by the manufacturer tests all aspects of device operation. Extensive testing of all programmable cells in the device include margin testing, internal verify, and program retention during high-temperature bake. All DC and AC parameters are tested at hot and cold temperatures using a variety of worst-case logic and signal patterns. Functional tests include reprogramming each OLMC to all valid architectural configurations.

Register Preload

The register preload feature allows OLMC registers to be directly loaded with any desired data pattern. It also allows the present state of OLMC registers to be examined regardless of TRI-STATE control conditions. This simplifies testing of devices after programming. A device may be put into any desired register state at any point during the functional test sequence. The test sequence may then be resumed to verify proper next-state transitions. This allows complete verification of sequential logic circuits, including states that are normally impossible or difficult to reach. It may also shorten the overall test time significantly.

A typical functional test sequence would be to verify all possible state transitions for the device being tested. To verify these transitions requires the ability to set the state registers into an arbitrary "present state" value, and to set the device inputs to any arbitrary "present input" value. Once this is done, the state machine is then clocked into a new state, or "next state." The next state is then checked to validate the transition from the present state. In this way any state transition can be checked.

Register preload is not an operational mode and is not intended for board-level testing because elevated voltage levels must be applied to the device. The programming equipment normally provides the register preload capability as part of its functional test facility. Note that the testing of GAL devices after programming by the user may be considered unnecessary because all E^2CMOS GAL products are completely tested by the manufacturer, guaranteeing 100% post-programming functional yield.

The register preload algorithm is described for those users who wish to test programmed GAL devices using test equipment other than approved GAL programming equipment. As shown in the register preload waveform in *Figure 5,* the preload sequence must not begin until the normal power-up reset operation has completed (after time t_{RESET}). The device is placed into preload mode by raising the "PRLD" input (pin 13*) to voltage V_{IES}, as specified in the register preload specifications (Table I).

To preload the OLMC registers, a series of data bits are shifted into the device on the "S_{DIN}" input (pin 11*), one bit for each OLMC in which registered output has been selected. (Non-registered OLMCs are bypassed.) The shift sequence is clocked by the rising edge of the "D_{CLK}" input (pin 1*). The data stream is shifted in through the registered OLMC with the lowest corresponding pin number, and then "upward" through all remaining registered OLMCs in pin-number ascending order. Therefore, the first data bit in the series is ultimately loaded into the registered OLMC with the highest corresponding pin number, as shown in *Figure 4.*

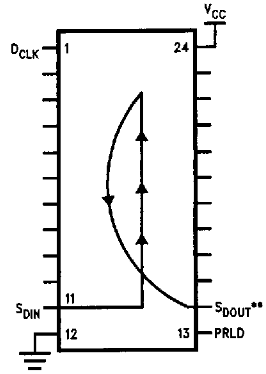
*Applies to 24-pin DIP packages for GAL22V10; refer to the 28-lead PCC Connection Diagram for conversion.

Register Preload (Continued)

As the data series is shifted into the S_{DIN} input, the contents of all registers (in registered OLMCs) are shifted "upward" and out onto the "S_{DOUT}" output (pin 14*). Complete present-state information can be examined in this manner. Test fixtures can be devised to test several GAL devices in which the S_{DOUT} pin of each chip is connected to the S_{DIN} pin of the next, and all preload and present-state data can be shifted around a single serial loop.

Note that when shifting register data into S_{DIN} or out of S_{DOUT}, V_{IL}/V_{OL} = register reset (0), and V_{IH}/V_{OH} = register set (1). These 0 and 1 register states are always inverted (active-low) on the normal output pins regardless of the selected output polarity (polarity affects logic function values before register inputs).

*Applies to 24-pin DIP packages for GAL22V10; refer to the 28-lead PCC Connection Diagram for conversion.



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**The S_{DOUT} output buffer is an open drain output during preload. This pin should be terminated to V_{CC} with a 10 kΩ resistor.

FIGURE 4. Output Register Preload Pinout

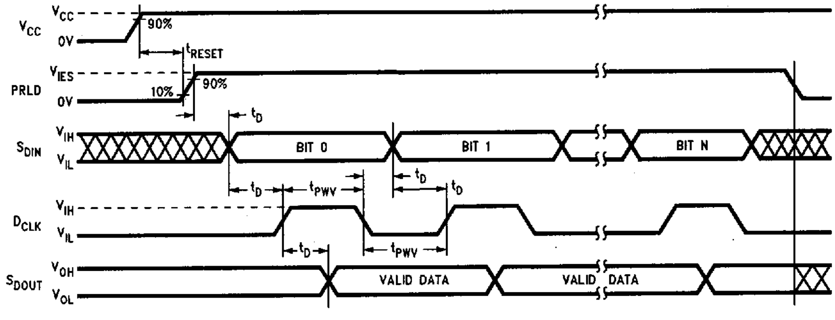
Register Preload Specifications

TABLE I

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IH}	Input Voltage (High)		2.40		V_{CC}	V
V_{IL}	Input Voltage (Low)		0.00		0.50	V
V_{IES}	Register Preload Input Voltage		14.5	15	15.5	V
V_{OH}	Output Voltage (High) (Note 1)				V_{CC}	V
V_{OL}	Output Voltage (Low) (Note 1)	$I_{OL} \le 12$ mA	0.00		0.50	V
I_{IH}, I_{IL}	Input Current (Programming)			±1	±10	μA
I_{OH}	High Level Output Current (Note 1)	$V_{OH} \le V_{CC}$			10	μA
t_{PWV}	Verify Pulse Width		1	5	10	μs
t_D	Pulse Sequence Delay		1	5	10	μs
t_{RESET}	Register Reset Time from Valid V_{CC}				45	μs

Note 1: The S_{DOUT} output buffer is an open drain output. This pin should be terminated to V_{CC} with a 10k resistor.

Register Preload Waveforms



TL/L/10406-19

FIGURE 5

OLMC Logic Diagram

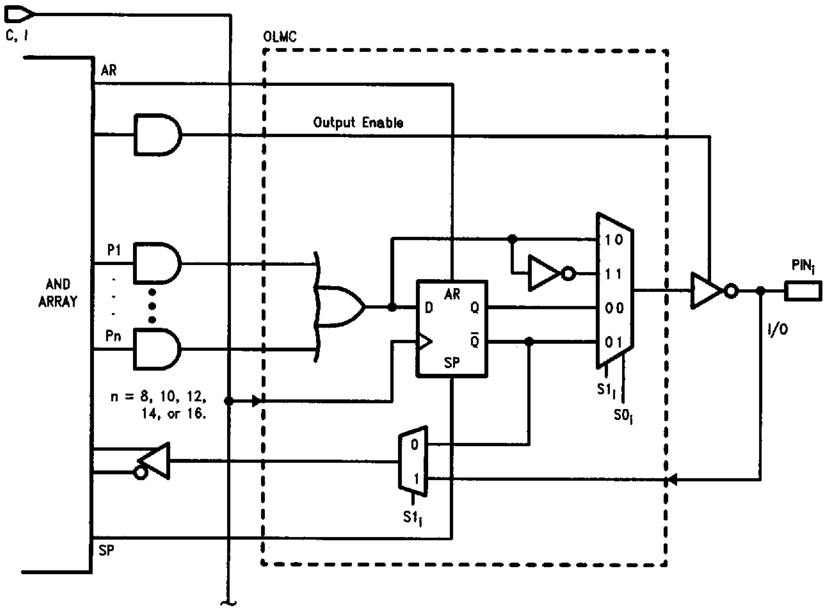


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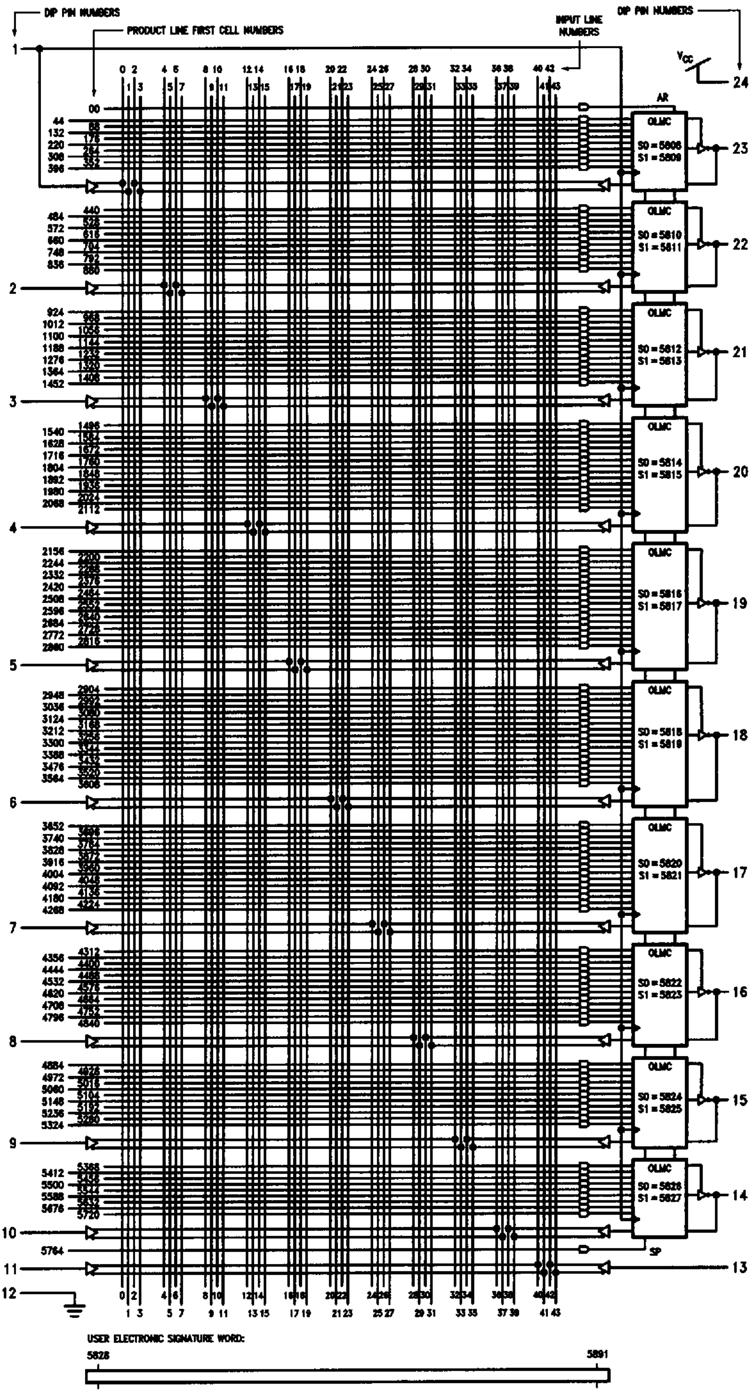
FIGURE 6

TABLE II

S1	S0	Output Configuration
0	0	Registered/Active Low
0	1	Registered/Active High
1	0	Combinatorial/Active Low
1	1	Combinatorial/Active High

GAL22V10 Logic Diagram



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JEDEC Logic Array Cell Numbers = Product Line First Cell Number + Input Line Numbers

FIGURE 7