SILERGY

Application Note:SY7901

High Efficiency 500kHz, 25V PWM Controller with DC Input Current Limit

General Description

SY7901 is a current mode DC/DC controller targeted for Boost, Sepic, Flyback and Forward applications. SY7901 has an accurate DC input current limit. External compensation provides flexible adjustment of control loops for different applications. The internal low side driver is capable of sourcing 1.5A and sinking 3A current.

Ordering Information

SY7901 □(□□)□
- └ Temperature Code
- Package Code
- Optional Spec Code

Ordering Number	Package type	Note
SY7901DBC	DFN3x3-10	----

Features

- Input voltage range 3V to 25V
- 500kHz fixed switching frequency
- An Accurate DC input current limit
- External compensation
- Internal softstart limits the inrush current
- Integrated low side driver: 1.5A sourcing and 3A sinking
- RoHS Compliant and Halogen Free
- Compact package: DFN3x3-10

Applications

- GPS Navigation Systems
- Handheld Devices
- Portable Media Player

Typical Applications

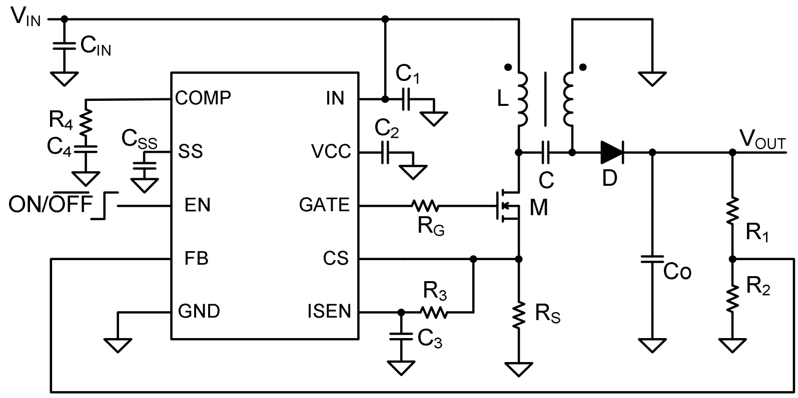
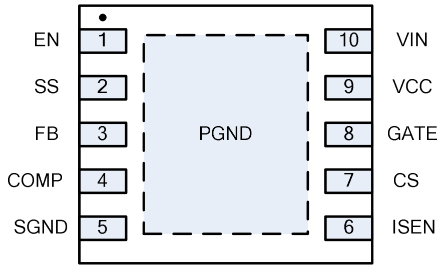


Figure 1. Schematic Diagram

Pinout (top view)



(DFN3x3-10)

Top Mark: FR*xyz* for SY7901 (Device code:FR, ***x=year code, y=week code, z= lot number code*)

Pin Name	Pin Number	Pin Description
VIN	10	Input pin. Decouple this pin to PGND pin with at least 1uF ceramic capacitor
VCC	9	5V Internal LDO output from VIN. Connect a 4.7 uF capacitor from this pin to PGND
GATE	8	Driver pin. Connect the gate of the power NFET to this pin
CS	7	Current sense pin. Connect an external current sensing resistor R_S from this pin to GND. The voltage on this pin is used to provide mosfet current feedback in the control loop and cycle by cycle peak current limit. Peak current limit is triggered when the sensed voltage plus the slope compensation exceed 340mV
ISEN	6	Connect this pin to CS to program the input average current limit. The input current limit should be I_{iLIM}=100mV/Rs
SGND	5	Signal ground pin
COMP	4	External compensation pin. Connect RC network from this pin to SGND to compensate the control loop
FB	3	Output voltage feedback pin. Connect this pin to the output voltage divider to program output voltage: Vout=1V*(1+R1/R2)
SS	2	Connect a capacitor from this pin to SGND to program the soft start time
EN	1	Enable pin. Pull it high to turn on the chip. Do not float this pin
PGND	Exposed Paddle	Power Ground Pin.

Absolute Maximum Ratings (Note 1)

IN,EN -- 26V
GATE -- VCC+0.3V
All other pins --- 6V
Power Dissipation, P_D @ T_A = 25°C, DFN3x3-10-- 2.6W
Package Thermal Resistance (Note 2)
θ_{JA} -- 38°C/W
θ_{JC} -- 130°C/W
Junction Temperature Range --- 125°C
Lead Temperature (Soldering, 10 sec.) -- 260°C
Storage Temperature Range -- -65°C to 150°C

Recommended Operating Conditions (Note 3)

IN-- 3V to 25V
Junction Temperature Range --- -40°C to 125°C
Ambient Temperature Range --- -40°C to 85°C

Electrical Characteristics

(V_{IN} = 12V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input Voltage Range	V_{IN}		3		25	V
Quiescent Current	I_Q	FB=1.1V		170		uA
Shutdown Current	I_{SHDN}	EN=0		0.1		uA
Feedback Reference Voltage	V_{REF}		0.98	1	1.02	V
FB Input Current	I_{FB}	V_{FB}=V_{IN}	-50		50	nA
Current Sense Limit	ISEN		98	100	102	mV
Internal Slope Compensation	V_{SLOPE}			40		mV/uS
Gm of EA	Gm			60		uA/V
Gate Driver Output Peak Current	I_{SOURCE}			1.5		A
	I_{SINK}			3		A
EN Rising Threshold	V_{ENH}		1.5			V
EN Falling Threshold	V_{ENL}				0.4	V
Input UVLO threshold	V_{UVLO}				2.9	V
UVLO hysteresis	V_{HYS}			0.3		V
Oscillator Frequency	F_{OSC}			500		kHz
Min On Time				200		ns
Min Off Time				200		ns
Internal LDO Output	V_{VCC}	V_{IN}=5.5V	4.9	5	5.1	V
Thermal Shutdown	T_{SD}			150		℃
Thermal Hysteresis	T_{HYST}			20		℃

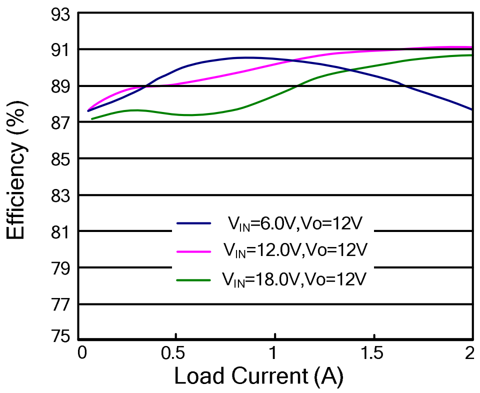
Note 1: Stresses beyond "Absolute Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: θ_{JA} is measured in the natural convection at TA = 25°C on a low effective single layer thermal conductivity test board of JEDEC 51-3 thermal measurement standard. Test condition: Device mounted on 2" x 2" FR-4 substrate PCB, 2oz copper, with minimum recommended pad on top layer and thermal vias to bottom layer ground plane.

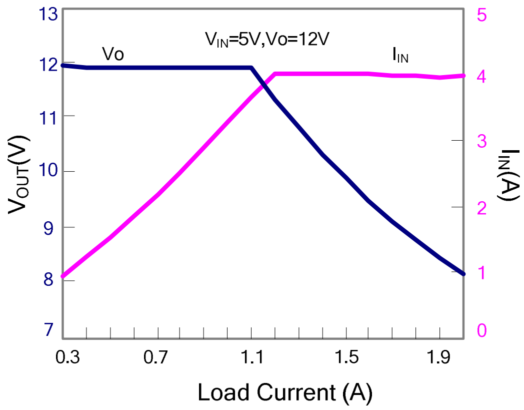
Note 3: The device is not guaranteed to function outside its operating conditions.

Typical Performance Characteristics

Efficiency vs. Load Current

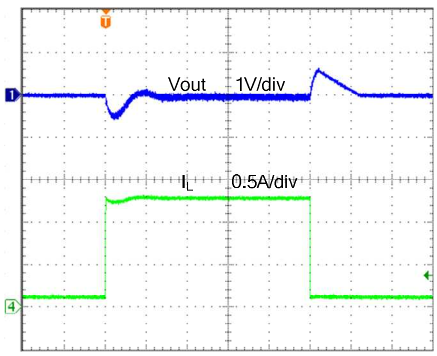


Input Current Limit



Load Transient

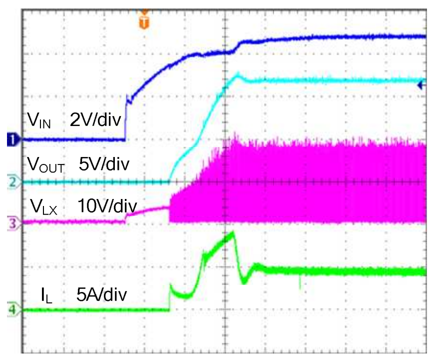
V_{IN}=5.0V, V_{OUT}=12V, Io=0.1~1.3A



Time (1mS/div)

Startup from V_{IN}

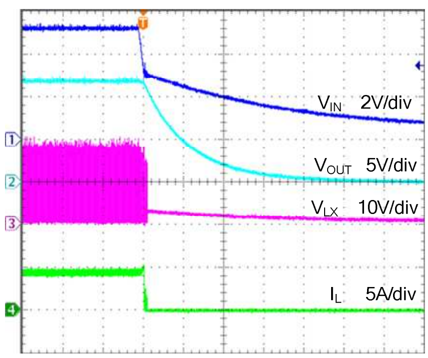
V_{IN}=5.0V, Io=1.0A



Time (2mS/div)

Startup from V_{IN}

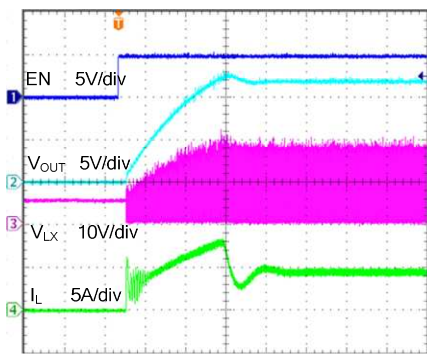
V_{IN}=5.0V, Io=1.0A



Time (2mS/div)

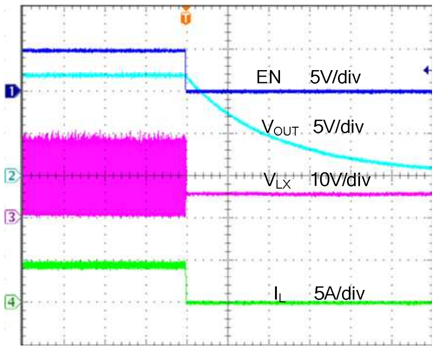
Startup from Enable

V_{IN}=5.0V, Io=1.0A



Time (1mS/div)

Shutdown from Enable
V_{IN}=5.0V, Io=1.0A



Time (1mS/div)

Operation

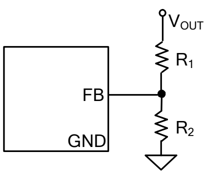
SY7901 is a current mode DC/DC controller targeted for Boost, Sepic, Flyback and Forward applications. SY7901 has an accurate DC input current limit. External compensation provides flexible adjustment of control loops for different applications. The internal low side driver is capable of sourcing 1.5A and sinking 3A current. It adopts constant frequency peak current mode control to ensure reliable over current protection and cycle by cycle switch current limit. The input current limit control senses the dc input current via a sense resistor and compares it against the internal threshold. If the input current is below the threshold, the IC operates under the constant output voltage operation mode and the output voltage is regulated by the feedback voltage sensed on the Vout. If the input current meets the threshold, the IC operates in the constant input current mode and the average input current is regulated to a level programmed by the input current sense resistor.

Applications Information

Feedback resistor dividers R_1 and R_2:

Choose R1 and R2 to program the output voltage under CV mode. To minimize the power consumption under light loads, it is desirable to choose large resistance values for both R1 and R2. A value of between 1k and 100k is highly recommended for R2. If R2=30k is chosen, then R1 can be calculated to be:

$$R1 = \frac{(V_{OUT} - 1V) \times R2}{1V}$$



Peak Current Sense Resistor

An external sensing resistor Rs is used to sense the current flow through the MOSFET. The sensed voltage is for peak current mode control and cycle by cycle peak current limit. Peak current limit will be triggered when the voltage on CS pin plus the internal slop compensation exceed 340mV, which is the typical clamping voltage of the PWM comparator. It is desirable to make the maximum value of sensing voltage plus the slope compensation to be about 70% of the clamping voltage during normal operation. Thus,

$$Rs = \frac{70\% \times 0.34 - Vslope \times D \times Ts}{I_{PEAK}}$$

Vslope is the slew rate of the internal compensation, I_{PEAK} is the peak current through MOSFET.

DC Current Limit

There are two feedback loops inside the controller. When the voltage on ISEN pin meets 100mV threshold, the current feedback loop will take over and regulate the output DC current to the target value. The reference voltage of current feedback loop will be affected by FB pin voltage. When the FB pin voltage is greater than 0.5V, the reference voltage is 100mV. When the FB pin voltage changes from 0.5V to 0.15V, the reference voltage will be changed from 100mV to 30mV.

Diode

Average current flowing through the diode is equal to the output current, so the diode current rating should be larger than the maximum output current. Reverse voltage of the diode is equal to Vin plus Vo, so the reverse voltage of the diode should be selected to be larger than the maximum value of Vin plus Vo. It is better to select a schottky diode to reduce the reverse recovery loss.

Power MOS

when Power MOS is turned off, the drain to source voltage is equal to Vin plus Vo, so the break down voltage of Power MOS should be larger than the maximum value of Vin plus Vo. When power MOS is turned off,a voltage spike is always generated due to the parasitic inductance, so voltage rating safe margin should be taken into consideration.

Output inductor L for Sepic Design:

Coupled inductor is recommended for sepic application to reduce the passive component size. Choose proper inductance to achieve desired current ripple. It is suggested to choose current ripple to be 40% of the maximum value of input current plus output current. Current rating of the inductor should be larger than 1.2*(Iin_max+Io_max). The inductance is calculated as:

$$L = \frac{V_{IN} \times V_O}{40\% \times F_{SW} \times (I_{OUT} + I_{IN})(V_{IN} + V_O)}$$

Other Application Examples

Figure 2 to 5 show other application examples of using SY7901.

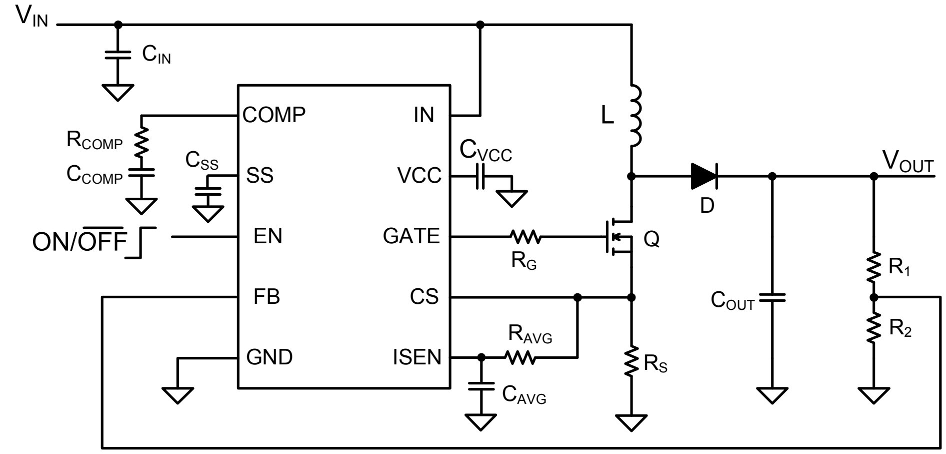


Figure 2. Boost with Power MOS Current Limit

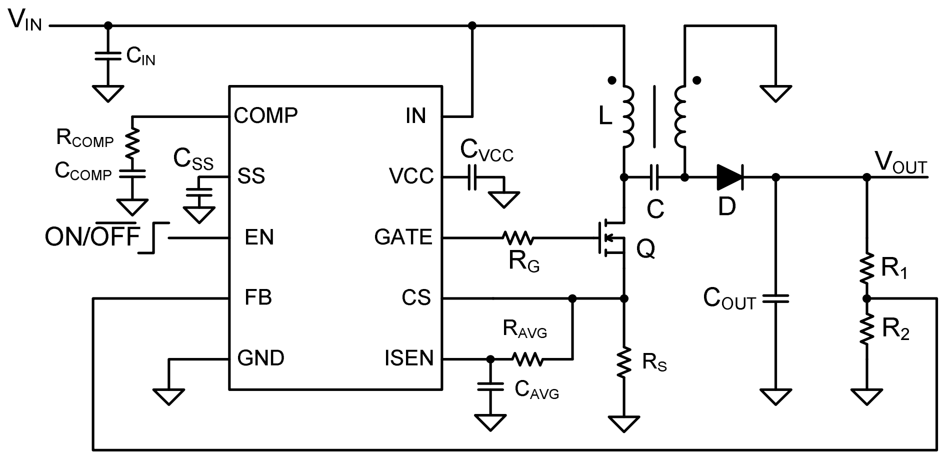


Figure 3. Sepic with Input Current Limit

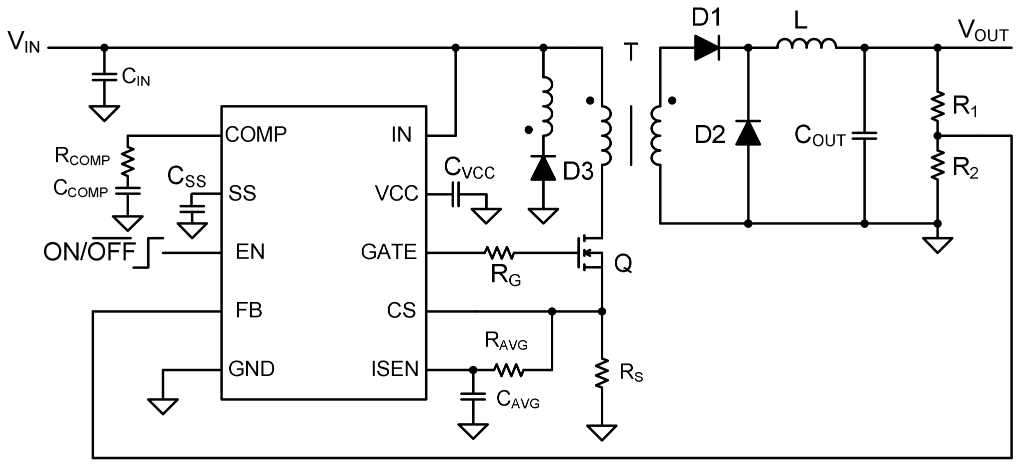


Figure 4 Forward with Input Current Limit

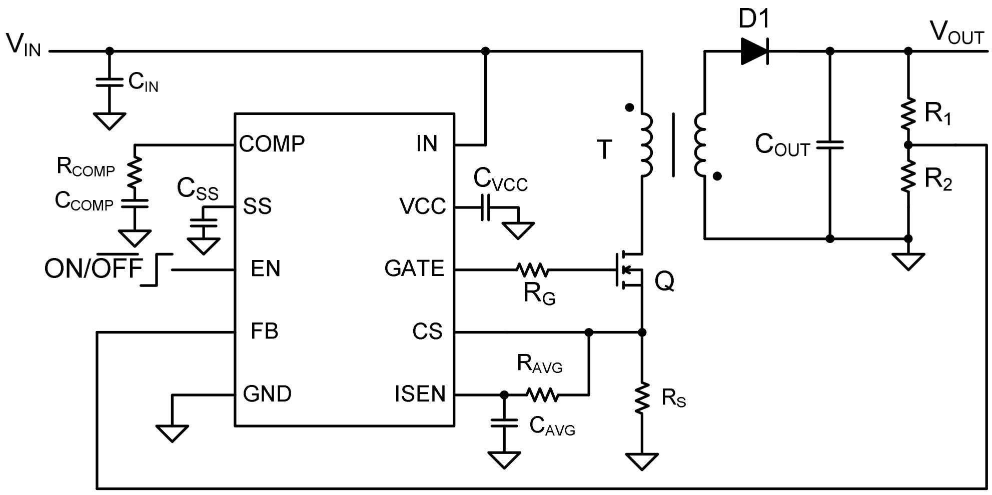
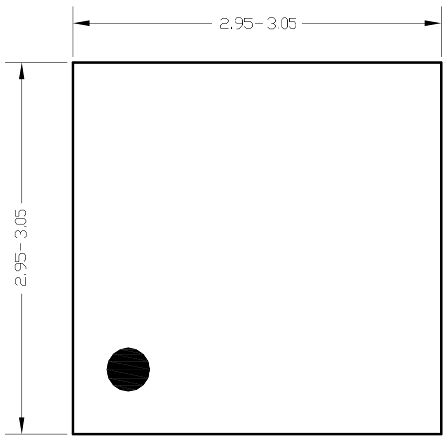
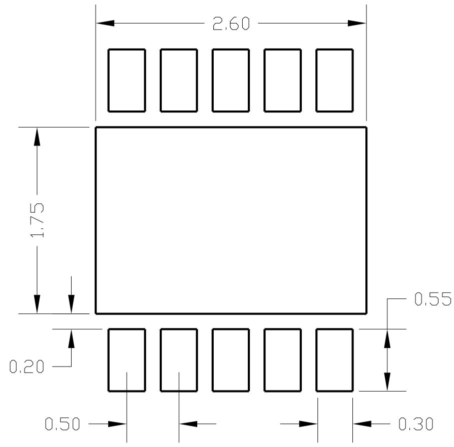


Figure 5 Flyback with Input Current Limit

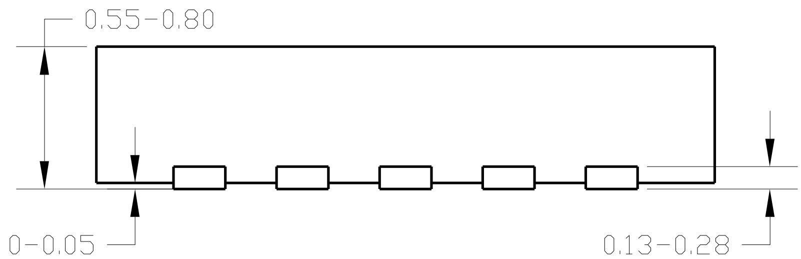
DFN3x3-10 Package outline



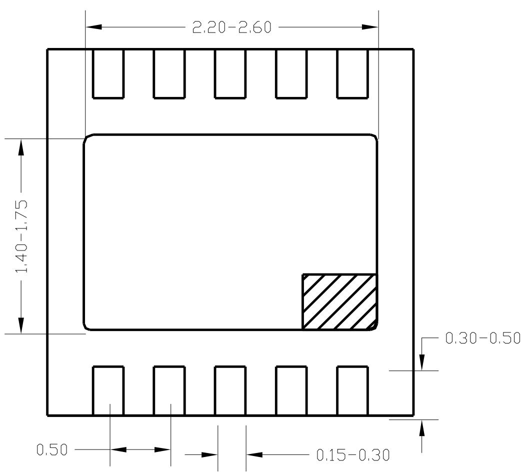
Top View

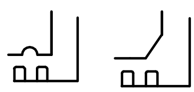


PCB layout (recommended)



Side View





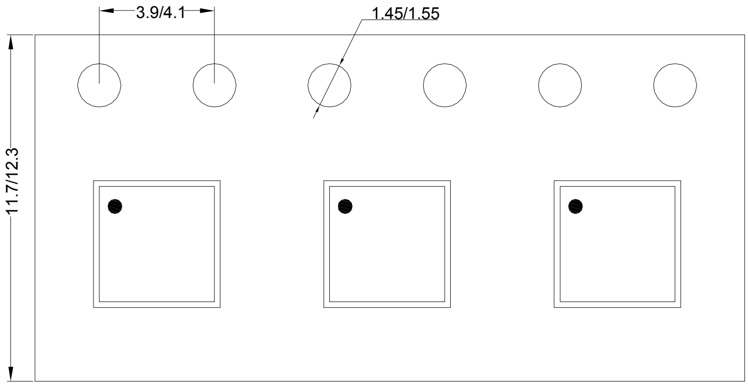
Detail A
Pin1 identifier: two options

Bottom View

Notes: All dimensions are in millimeters and exclude mold flash & metal burr.

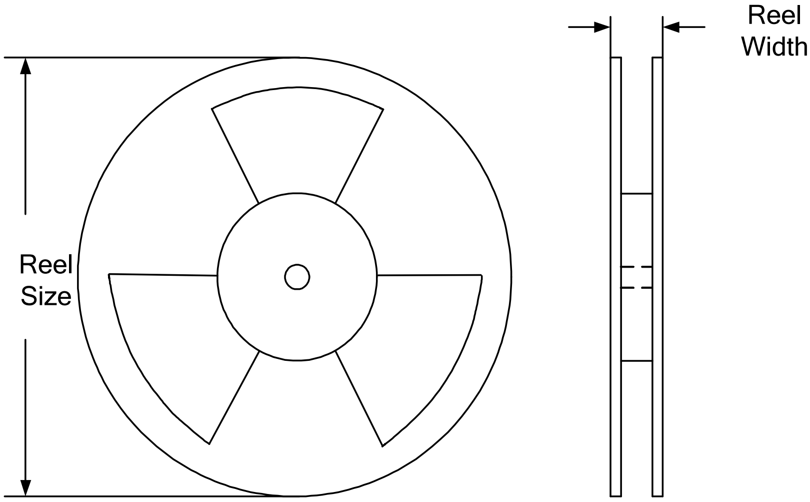
Taping & Reel Specification

1. DFN3x3-10 taping orientation



Feeding direction →

2. Carrier Tape & Reel specification for packages



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Reel width(mm)	Trailer length(mm)	Leader length (mm)	Qty per reel
DFN3x3	10	8	13"	12.4	400	400	5000