Data Sheet | June 28, 2007 | FN6377.1

34µA Micro-power Single and Dual Precision Rail-to-Rail Input-Output (RRIO) Low Input Bias Current Op Amps

The ISL28158 and ISL28258 are micro-power precision operational amplifiers optimized for single supply operation at 5.5V and can operate down to 2.4V.

These devices feature an Input Range Enhancement Circuit (IREC) which enables them to maintain CMRR performance for input voltages greater than the positive supply. The input signal is capable of swinging 0.25V above the positive supply and to 100mV below the negative supply with only a slight degradation of the CMRR performance. The output operation is rail-to-rail.

The ISL28158 and ISL28258 draw minimal supply current while meeting excellent DC-accuracy noise and output drive specifications. Competing devices seriously degrade these parameters to achieve micro-power supply current. Offset current, voltage and current noise, slew rate, and gain-bandwidth product are all two to ten times better than on previous micro-power op amps.

The 1/f corner of the voltage noise spectrum is at 100Hz. This results in low frequency noise performance which can only be found on devices with an order of magnitude higher supply current.

ISL28158 and ISL28258 can be operated from one lithium cell or two Ni-Cd batteries. The input range includes both positive and negative rail. The output swings to both rails.

Ordering Information

PART NUMBER (Note)	PART MARKING	PACKAGE (Pb-free)	PKG. DWG. #
ISL28158FHZ-T7*	GABW	6 Ld SOT-23	MDP0038
ISL28158FHZ-T7A*	GABW	6 Ld SOT-23	MDP0038
ISL28158FBZ	28158 FBZ	8 Ld SOIC	MDP0027
ISL28158FBZ-T7*	28158 FBZ	8 Ld SOIC	MDP0027
Coming Soon ISL28258FBZ-T7*		8 Ld SOIC	MDP0027
Coming Soon ISL28258FAZ-T7*		8 Ld MSOP	MDP0043

*Add “-T7” or “-T7A” suffix for tape and reel. Please refer to TB347 for details on reel specifications.

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Features

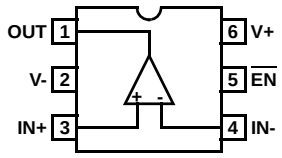
- 34µA typical supply current
- 300µV maximum offset voltage (8 Ld SOIC)
- 1pA typical input bias current
- 200kHz gain bandwidth product
- 2.4V to 5.5V single supply voltage range
- Rail-to-rail input and output
- Enable pin (ISL28158 only)
- Pb-free plus anneal available (RoHS compliant)

Applications

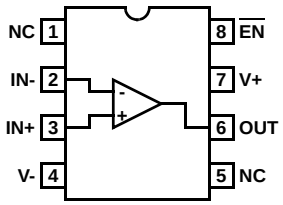
- Battery- or solar-powered systems
- 4mA to 20mA current loops
- Handheld consumer products
- Medical devices
- Sensor amplifiers
- ADC buffers
- DAC output amplifiers

Pinouts

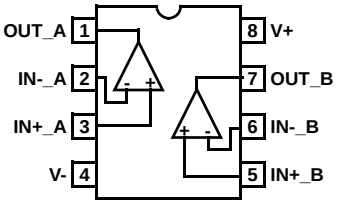
ISL28158 (6 LD SOT-23) TOP VIEW



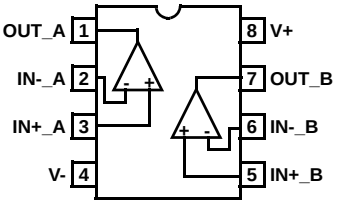
ISL28158 (8 LD SOIC) TOP VIEW



ISL28258 (8 LD SOIC) TOP VIEW



ISL28258 (8 LD MSOP) TOP VIEW



Absolute Maximum Ratings (T_A = +25°C)

Supply Voltage 5.75V
Supply Turn On Voltage Slew Rate 1V/µs
Differential Input Current 5mA
Differential Input Voltage 0.5V
Input Voltage . . . . . V- -0.5V to V+ +0.5V
ESD Rating
Human Body Model 3kV
Machine Model 300V

Thermal Information

Thermal Resistance	θ_{JA} (°C/W)
6 Ld SOT-23 Package	230
8 Ld SOIC Package	110
8 Ld MSOP Package	115

Output Short-Circuit Duration . . . . . .Indefinite
Ambient Operating Temperature Range . . . . . .-40°C to +125°C
Storage Temperature Range . . . . . .-65°C to +150°C
Operating Junction Temperature . . . . . .+125°C
Pb-free reflow profile . . . . . .see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typical values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$

Electrical Specifications

V+ = 5V, V- = 0V, V_{CM} = 2.5V, R_L = Open, T_A = +25°C unless otherwise specified. **Boldface limits apply over the operating temperature range, -40°C to +125°C.** Temperature data established by characterization.

PARAMETER	DESCRIPTION	CONDITIONS	MIN (Note 1)	TYP	MAX (Note 1)	UNIT
DC SPECIFICATIONS						
V_{OS}	Input Offset Voltage	8 Ld SOIC	-300 **-650**	3.1	300 **650**	µV
		6 Ld SOT-23	-550 **-750**	5	550 **750**	
$\frac{\Delta V_{OS}}{\Delta T}$	Input Offset Voltage vs Temperature			0.3		µV/°C
I_{OS}	Input Offset Current	T_A = -40°C to +85°C	-35 **-80**	±5	35 **80**	pA
I_B	Input Bias Current	T_A = -40°C to +85°C	-30 **-80**	±1	30 **80**	pA
V_{CM}	Common-Mode Voltage Range	Guaranteed by CMRR	0		5	V
CMRR	Common-Mode Rejection Ratio	V_{CM} = 0V to 5V	75 **70**	98		dB
PSRR	Power Supply Rejection Ratio	V_+ = 2.4V to 5.5V	80 **75**	98		dB
A_{VOL}	Large Signal Voltage Gain	V_O = 0.5V to 4.5V, R_L = 100kΩ to V_{CM}	100 **75**	220		V/mV
		V_O = 0.5V to 4.5V, R_L = 1kΩ to V_{CM}		45		V/mV
V_{OUT}	Maximum Output Voltage Swing	Output low, R_L = 100kΩ to V_{CM}		5.3	6 **20**	mV
		Output low, R_L = 1kΩ to V_{CM}		135	150 **250**	mV
		Output high, R_L = 100kΩ to V_{CM}	4.995 **4.993**	4.996		V
		Output high, R_L = 1kΩ to V_{CM}	4.84 **4.77**	4.874		V
$I_{S,ON}$	Quiescent Supply Current, Enabled	V_+ = 5V	26 **15**	34	43 **55**	µA
		V_+ = 2.4V		20		µA

Electrical Specifications $V+ = 5V$, $V- = 0V$, $V_{CM} = 2.5V$, R_L = Open, $T_A = +25°C$ unless otherwise specified. **Boldface limits apply over the operating temperature range, -40°C to +125°C.** Temperature data established by characterization. **(Continued)**

PARAMETER	DESCRIPTION	CONDITIONS	MIN (Note 1)	TYP	MAX (Note 1)	UNIT
$I_{S,OFF}$	Quiescent Supply Current, Disabled			10	14 **19**	µA
I_O+	Short-Circuit Output Source Current	$R_L = 10\Omega$ to V_{CM}	27 **20**	30		mA
I_O-	Short-Circuit Output Sink Current	$R_L = 10\Omega$ to V_{CM}	22 **15**	25		mA
V_{SUPPLY}	Supply Operating Range	V_+ to V_-	2.4		5.5	V
V_{ENH}	$\overline{EN}$ Pin High Level		**2**			V
V_{ENL}	$\overline{EN}$ Pin Low Level				**0.8**	V
I_{ENH}	$\overline{EN}$ Pin Input High Current	$V_{\overline{EN}} = V_+$		1	1.5 **1.6**	µA
I_{ENL}	$\overline{EN}$ Pin Input Low Current	$V_{\overline{EN}} = V_-$		12	25 **30**	nA
AC SPECIFICATONS						
GBW	Gain Bandwidth Product	$A_V = 100$, $R_F = 100k\Omega$, $R_G = 1k\Omega$, $R_L = 10k\Omega$ to V_{CM}		200		kHz
Unity Gain Bandwidth	-3dB Bandwidth	$A_V = 1$, $R_F = 0\Omega$, $V_{OUT} = 10mV_{P-P}$		420		kHz
e_N	Input Noise Voltage Peak-to-Peak	f = 0.1Hz to 10Hz		1.4		μV_{PP}
	Input Noise Voltage Density	f_O = 1kHz		64		$nV/\sqrt{Hz}$
i_N	Input Noise Current Density	f_O = 10kHz		0.19		$pA/\sqrt{Hz}$
CMRR @ 60Hz	Input Common Mode Rejection Ratio	$V_{CM} = 1V_{P-P}$, $R_L = 10k\Omega$ to V_{CM}		-70		dB
PSRR+ @ 120Hz	Power Supply Rejection Ratio (V_+)	V_+, V_- = ±1.2V and ±2.5V, $V_{SOURCE} = 1V_{P-P}$, $R_L = 10k\Omega$ to V_{CM}		-64		dB
PSRR- @ 120Hz	Power Supply Rejection Ratio (V_-)	V_+, V_- = ±1.2V and ±2.5V $V_{SOURCE} = 1V_{P-P}$, $R_L = 10k\Omega$ to V_{CM}		-85		dB
TRANSIENT RESPONSE						
SR	Slew Rate			0.1		V/µs
t_r, t_f, Large Signal	Rise Time, 10% to 90% V_{OUT}	$A_V = +2$, $V_{OUT} = 1V_{P-P}$, $R_g = R_f = 10k\Omega$ $R_L = 10k\Omega$ to V_{CM}		10		µs
	Fall Time, 90% to 10% V_{OUT}	$A_V = +2$, $V_{OUT} = 1V_{P-P}$, $R_g = R_f = 10k\Omega$ $R_L = 10k\Omega$ to V_{CM}		9		µs
t_r, t_f, Small Signal	Rise Time, 10% to 90% V_{OUT}	$A_V = +2$, $V_{OUT} = 10mV_{P-P}$, $R_g = R_f = R_L = 10k\Omega$ to V_{CM}		650		ns
	Fall Time, 90% to 10% V_{OUT}	$A_V = +2$, $V_{OUT} = 10mV_{P-P}$, $R_g = R_f = R_L = 10k\Omega$ to V_{CM}		640		ns
$t_{\overline{EN}}$	Enable to Output Turn-on Delay Time, 10% $\overline{EN}$ to 10% V_{OUT}	$V_{\overline{EN}}$ = 5V to 0V, $A_V = +2$, $R_g = R_f = R_L$ = 1k to VCM		15		µs
	Enable to Output Turn-off Delay Time, 10% $\overline{EN}$ to 10% V_{OUT}	$V_{\overline{EN}}$ = 0V to 5V, $A_V = +2$, $R_g = R_f = R_L$ = 1k to V_{CM}		0.5		µs

NOTE:

1. Parts are 100% tested at +25°C. Over temperature limits established by characterization and are not production tested.

Typical Performance Curves $V+ = 5V, V- = 0V, V_{CM} = 2.5V, R_L = Open$

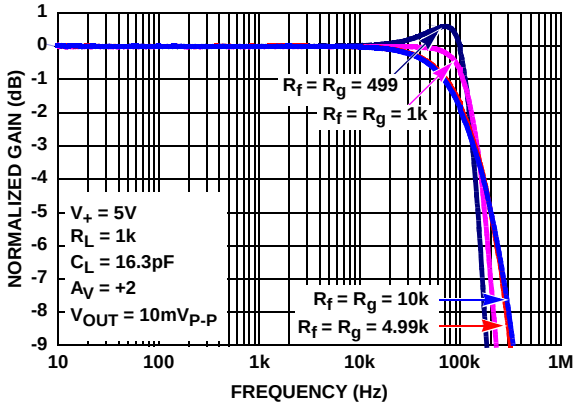


FIGURE 1. GAIN vs FREQUENCY vs FEEDBACK RESISTOR VALUES R_f/R_g

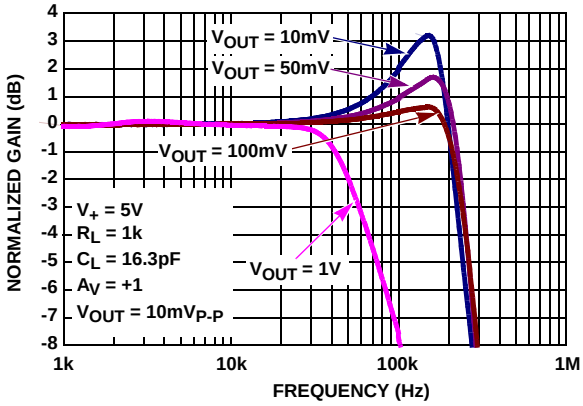


FIGURE 2. GAIN vs FREQUENCY vs V_{OUT}, R_L = 1k

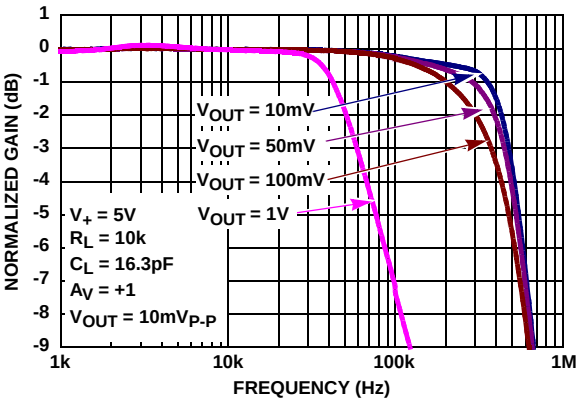


FIGURE 3. GAIN vs FREQUENCY vs V_{OUT}, R_L = 10k

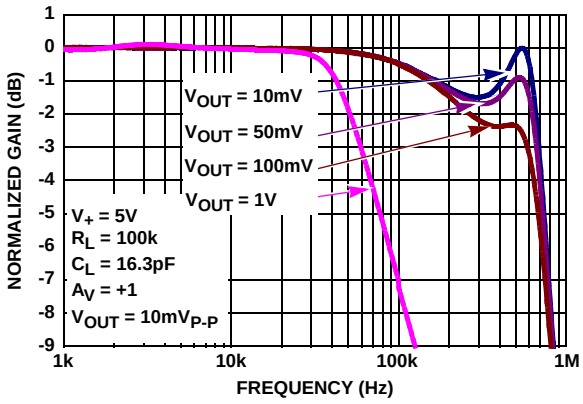


FIGURE 4. GAIN vs FREQUENCY vs V_{OUT}, R_L = 100k

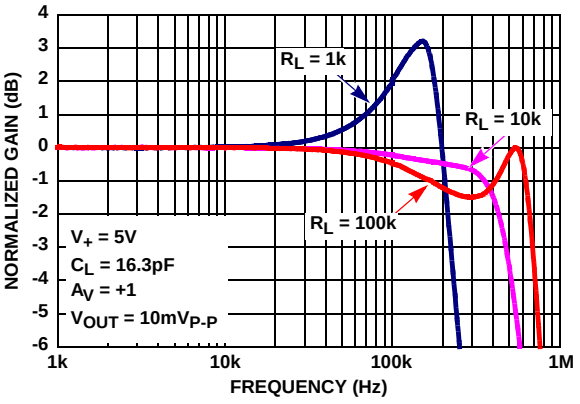


FIGURE 5. GAIN vs FREQUENCY vs R_L

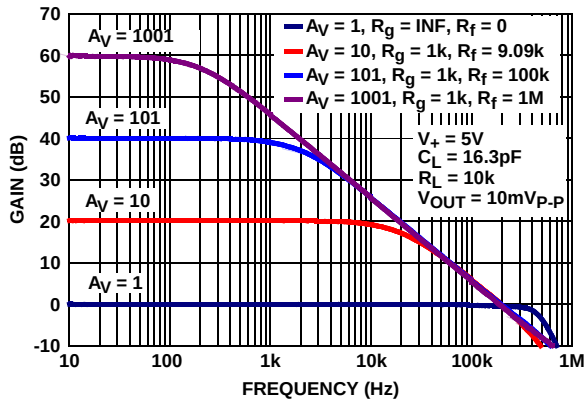


FIGURE 6. FREQUENCY RESPONSE vs CLOSED LOOP GAIN

Typical Performance Curves $V+ = 5V, V- = 0V, V_{CM} = 2.5V, R_L = Open$ **(Continued)**

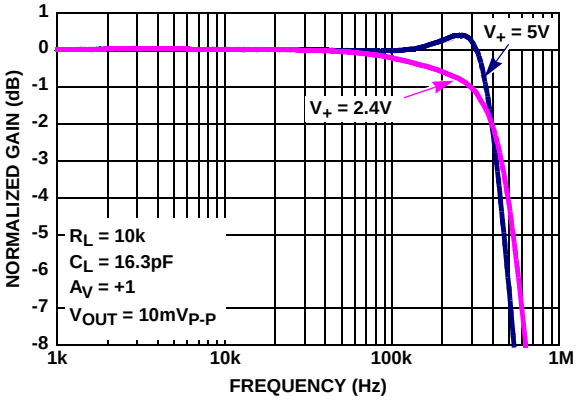


FIGURE 7. GAIN vs FREQUENCY vs SUPPLY VOLTAGE

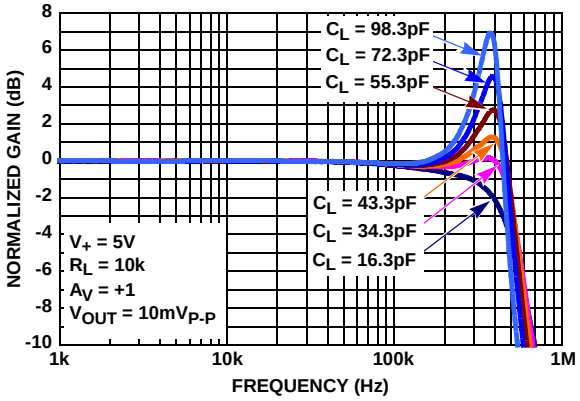


FIGURE 8. GAIN vs FREQUENCY vs C_L

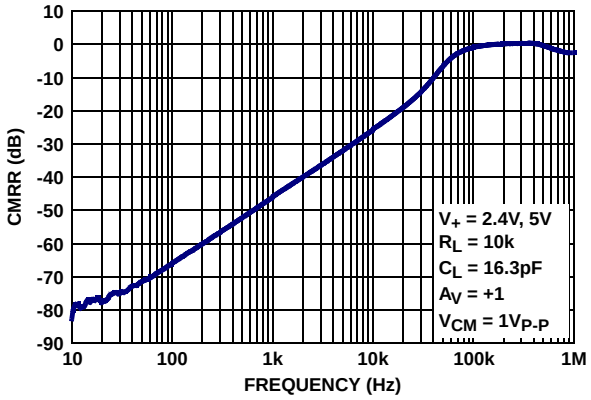


FIGURE 9. CMRR vs FREQUENCY, V_+ = 2.4V AND 5V

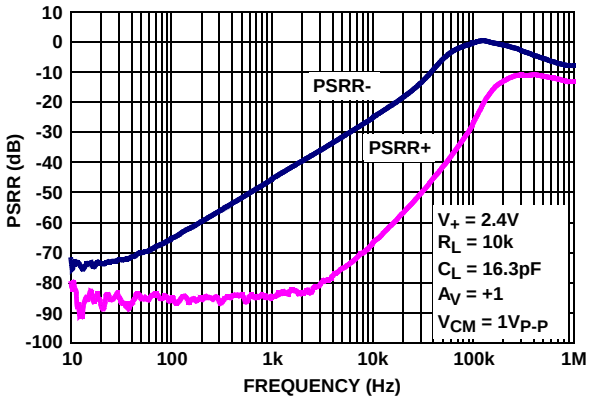


FIGURE 10. PSRR vs FREQUENCY, V_+, V_- = ±1.2V

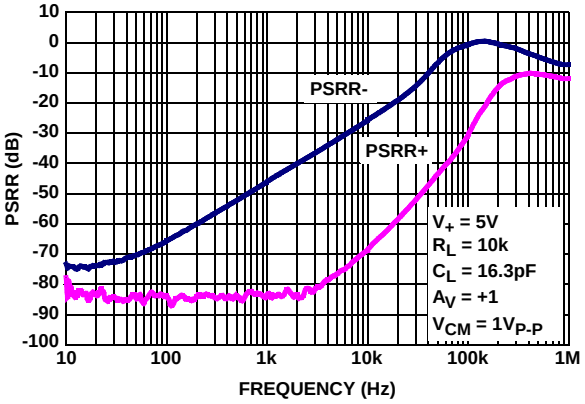


FIGURE 11. PSRR vs FREQUENCY, V_+, V_- = ±2.5V

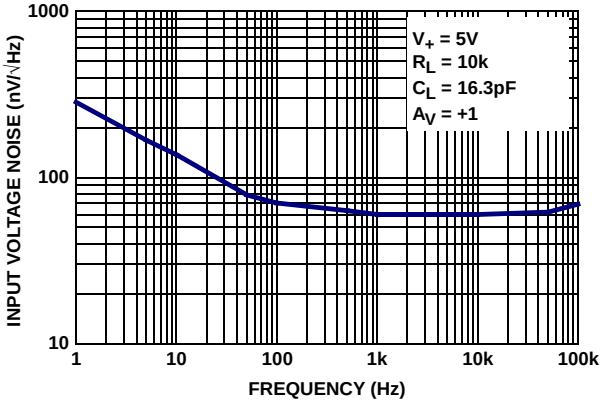


FIGURE 12. INPUT VOLTAGE NOISE DENSITY vs FREQUENCY

Typical Performance Curves $V+ = 5V, V- = 0V, V_{CM} = 2.5V, R_L$ = Open **(Continued)**

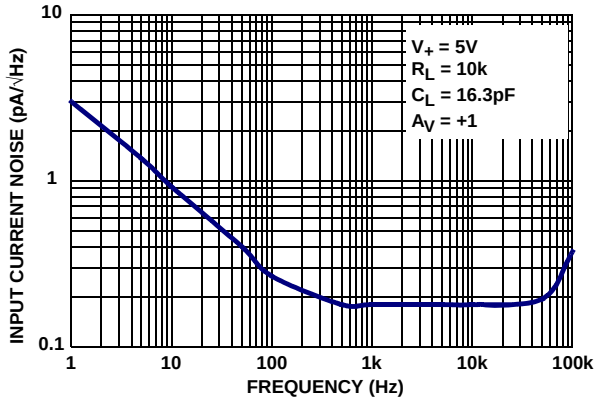


FIGURE 13. INPUT CURRENT NOISE DENSITY vs FREQUENCY

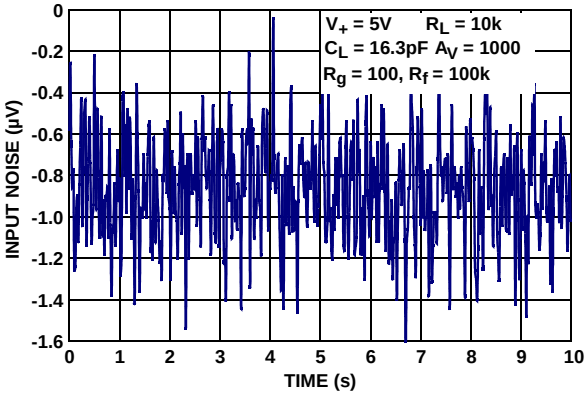


FIGURE 14. INPUT VOLTAGE NOISE 0.1Hz TO 10Hz

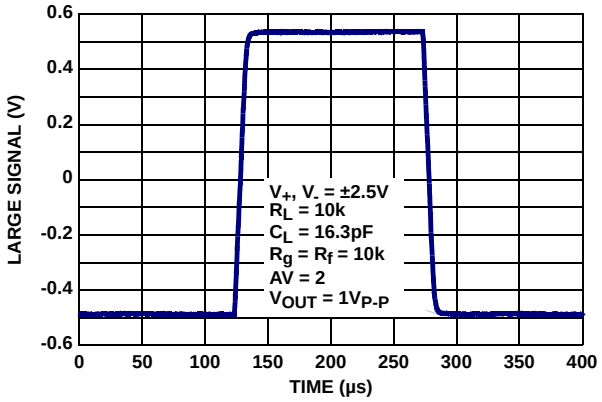


FIGURE 15. LARGE SIGNAL STEP RESPONSE

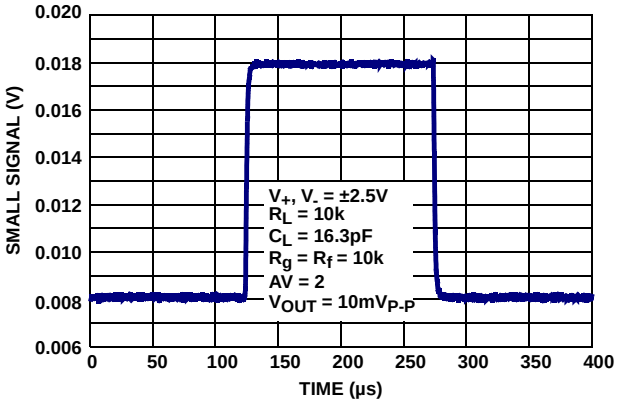


FIGURE 16. SMALL SIGNAL STEP RESPONSE

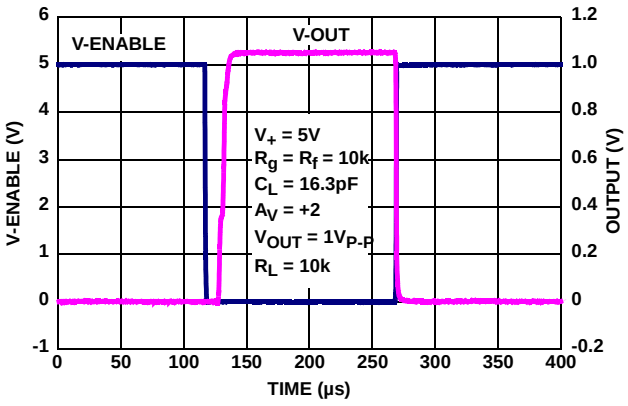


FIGURE 17. ENABLE TO OUTPUT RESPONSE

Typical Performance Curves $V+ = 5V, V- = 0V, V_{CM} = 2.5V, R_L$ = Open **(Continued)**

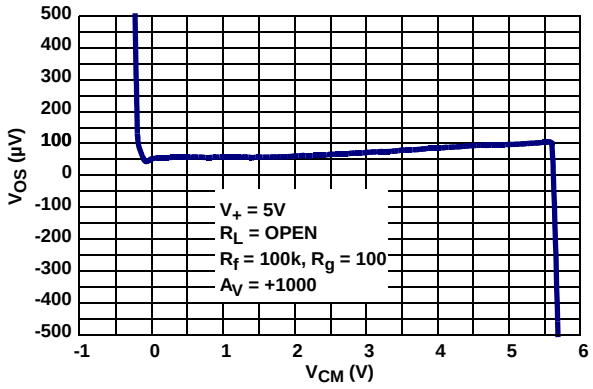


FIGURE 18. INPUT OFFSET VOLTAGE vs COMMON MODE INPUT VOLTAGE

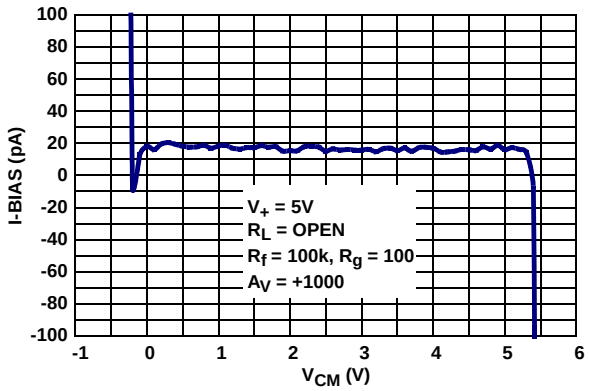


FIGURE 19. INPUT BIAS CURRENT vs COMMON MODE INPUT VOLTAGE

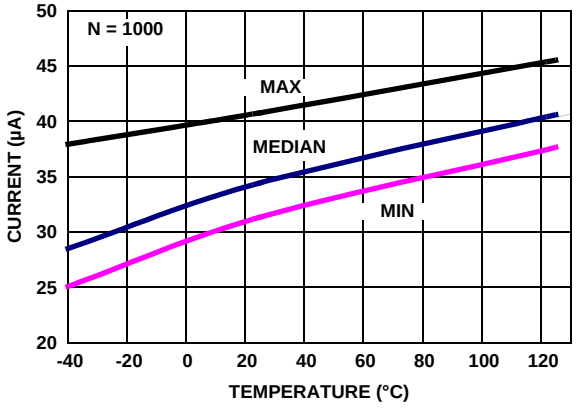


FIGURE 20. SUPPLY CURRENT ENABLED vs TEMPERATURE, V_+, V_- = ±2.5V

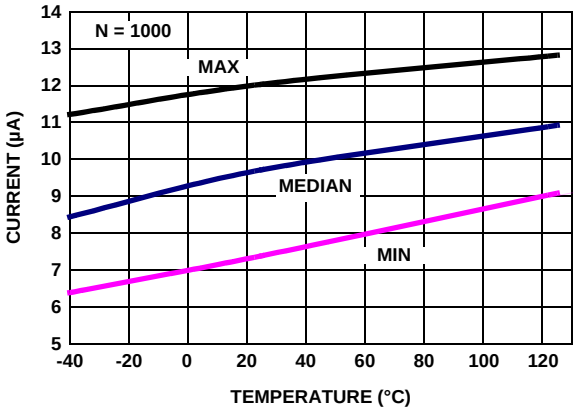


FIGURE 21. SUPPLY CURRENT DISABLED vs TEMPERATURE, V_+, V_- = ±2.5V

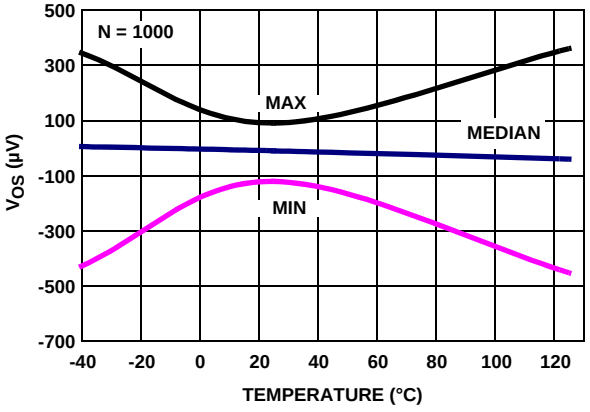


FIGURE 22. V_{OS} (SOIC PKG) vs TEMPERATURE, V_{IN} = 0V, V_+, V_- = ±2.75V

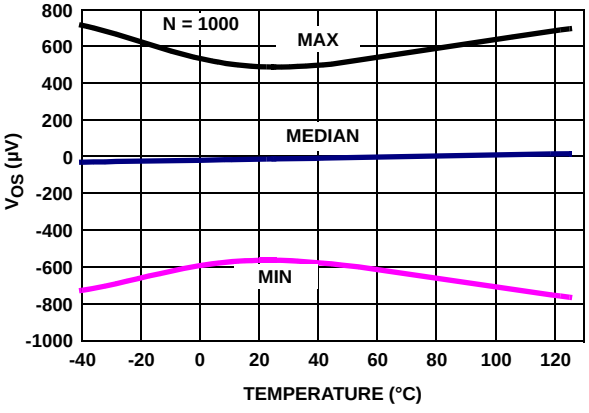


FIGURE 23. V_{OS} (SOT PKG) vs TEMPERATURE, V_{IN} = 0V, V_+, V_- = ±2.75V

Typical Performance Curves $V+ = 5V, V- = 0V, V_{CM} = 2.5V, R_L$ = Open **(Continued)**

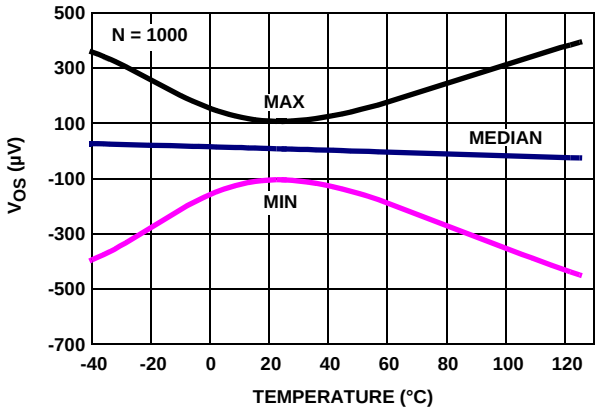


FIGURE 24. V_{OS} (SOIC PKG) vs TEMPERATURE, V_{IN} = 0V, V_+, V_- = ±2.5V

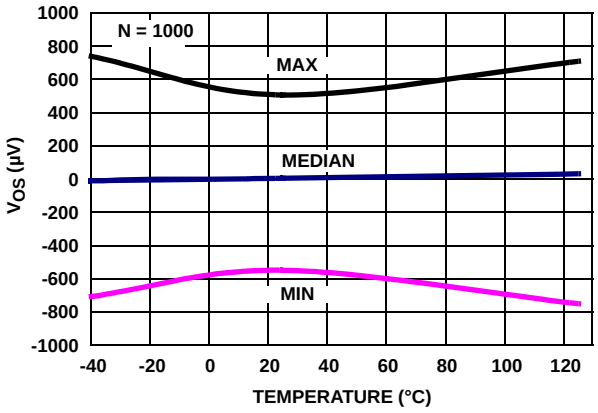


FIGURE 25. V_{OS} (SOT PKG) vs TEMPERATURE, V_{IN} = 0V, V_+, V_- = ±2.5V

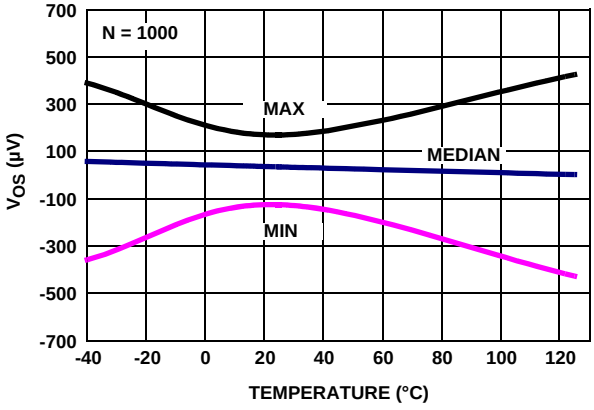


FIGURE 26. V_{OS} (SOIC PKG) vs TEMPERATURE, V_{IN} = 0V, V_+, V_- = ±1.2V

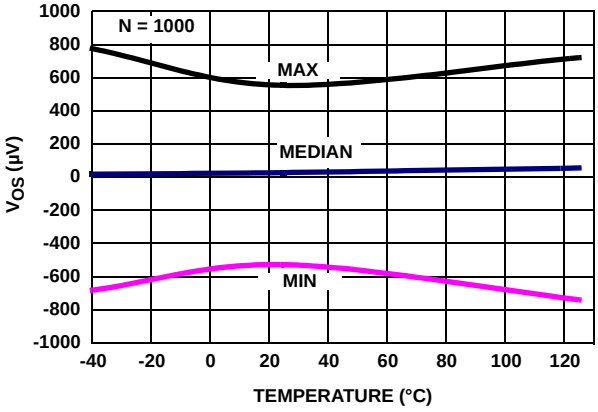


FIGURE 27. V_{OS} (SOT PKG) vs TEMPERATURE, V_{IN} = 0V, V_+, V_- = ±1.2V

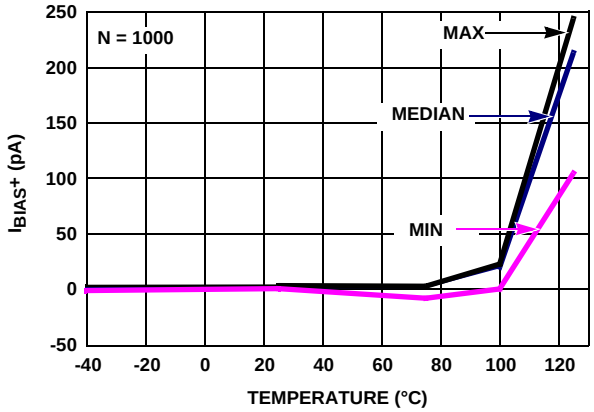


FIGURE 28. $I_{BIAS}+$ vs TEMPERATURE, V_+, V_- = ±2.5V

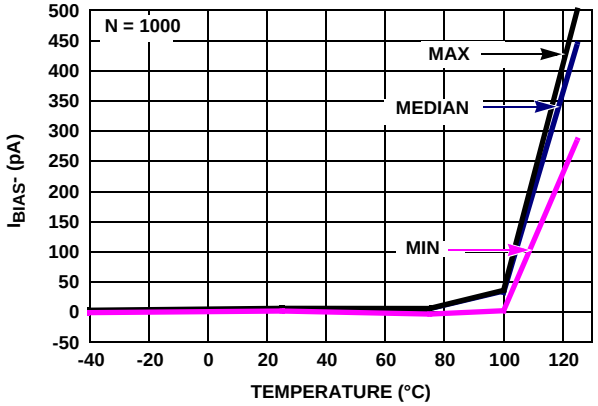


FIGURE 29. $I_{BIAS}-$ vs TEMPERATURE, V_+, V_- = ±2.5V

Typical Performance Curves $V+ = 5V, V- = 0V, V_{CM} = 2.5V, R_L$ = Open **(Continued)**

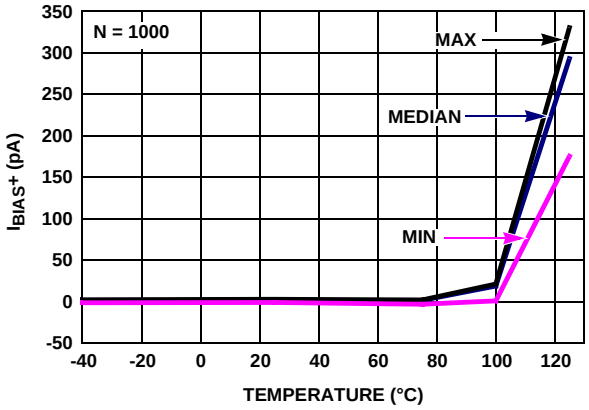


FIGURE 30. $I_{BIAS}+$ vs TEMPERATURE, V_+, V_- = ±1.2V

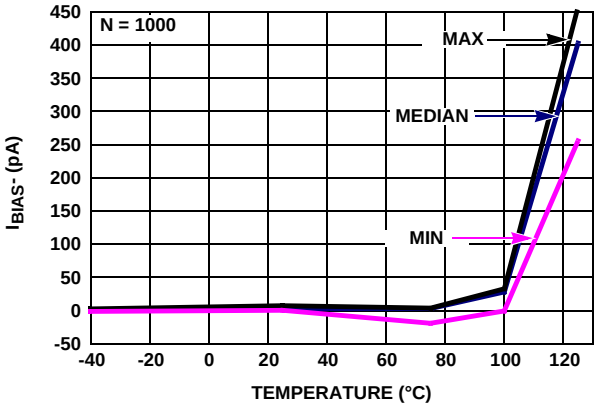


FIGURE 31. $I_{BIAS}-$ vs TEMPERATURE, V_+, V_- = ±1.2V

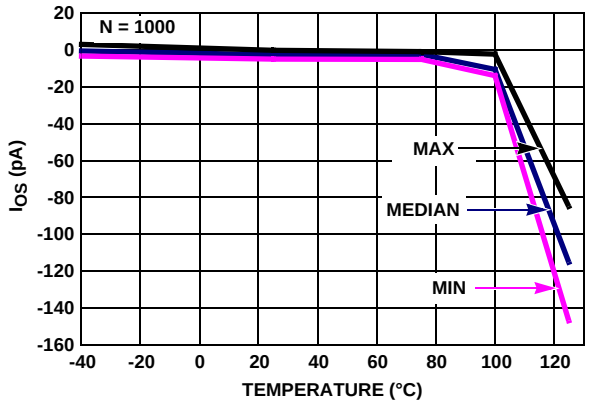


FIGURE 32. I_{OS} vs TEMPERATURE, V_+, V_- = ±2.5

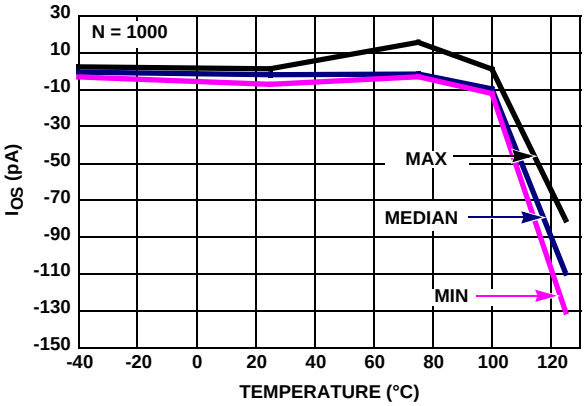


FIGURE 33. I_{OS} vs TEMPERATURE, V_+, V_- = ±1.2V

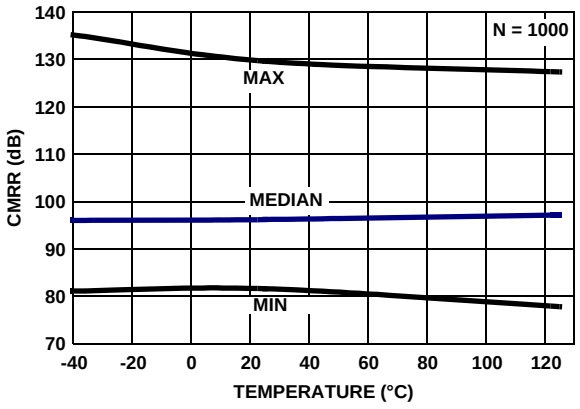


FIGURE 34. CMRR vs TEMPERATURE, V_{CM} = -2.5V TO +2.5V, V_+, V_- = ±2.5V

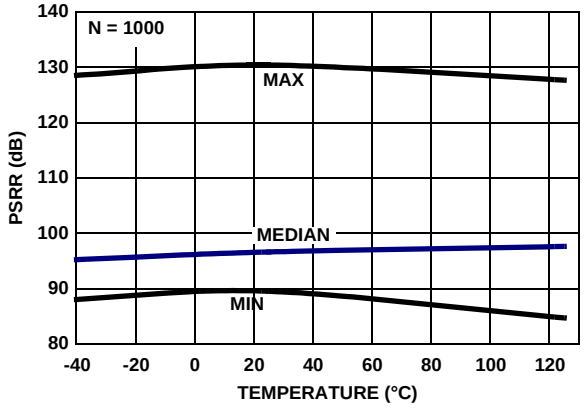


FIGURE 35. PSRR vs TEMPERATURE, V_+, V_- = ±1.2V TO ±2.75V

Typical Performance Curves V+ = 5V, V- = 0V, V_{CM} = 2.5V, R_L = Open (Continued)

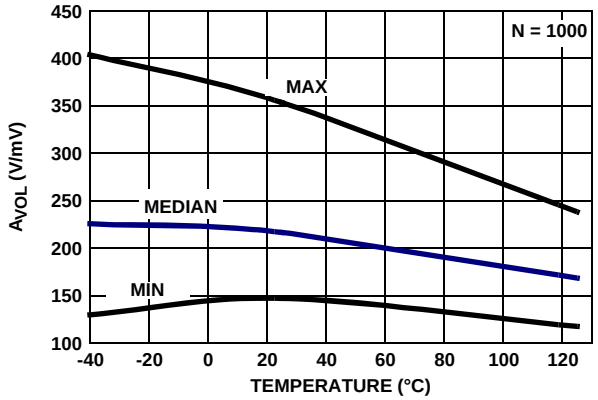


FIGURE 36. A_{VOL} vs TEMPERATURE, V_+, V_- = ±2.5V, V_O = -2V TO +2V, R_L = 100k

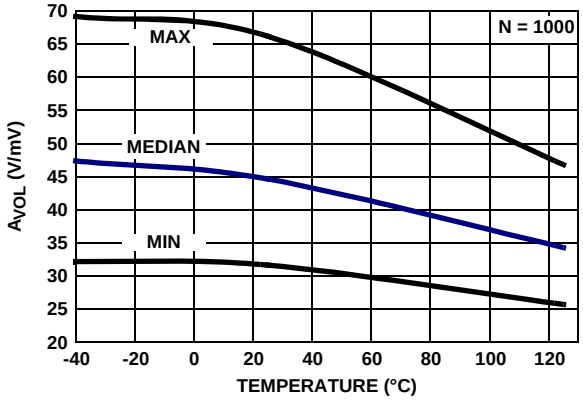


FIGURE 37. A_{VOL} vs TEMPERATURE, V_+, V_- = ±2.5V, V_O = -2V TO +2V, R_L = 1k

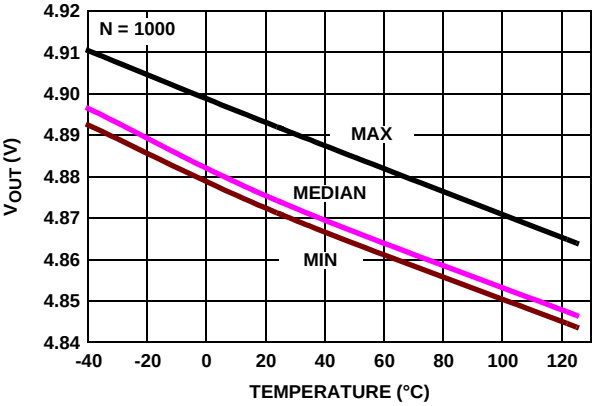


FIGURE 38. V_{OUT} HIGH vs TEMPERATURE, V_+, V_- =±2.5V, R_L = 1k

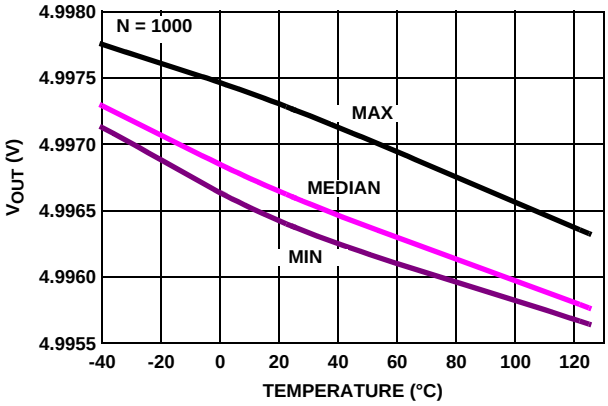


FIGURE 39. V_{OUT} HIGH vs TEMPERATURE, V_+, V_- = ±2.5V, R_L = 100k

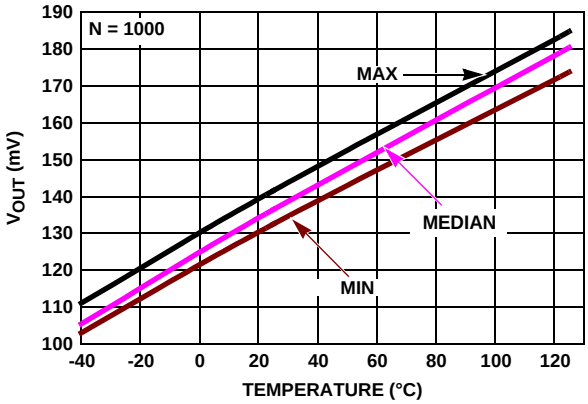


FIGURE 40. V_{OUT} LOW vs TEMPERATURE, V_+, V_- = ±2.5V, R_L = 1k

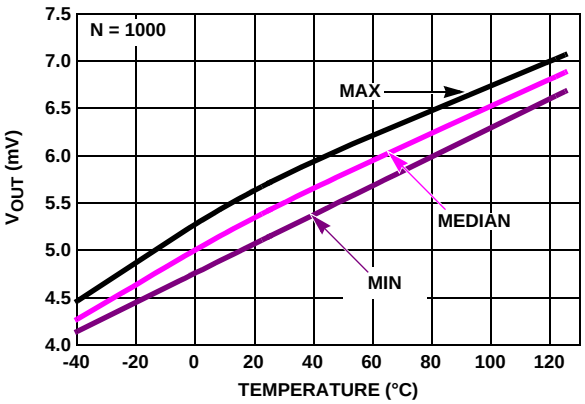


FIGURE 41. V_{OUT} LOW vs TEMPERATURE, V_+, V_- = ±2.5V, R_L = 100k

Typical Performance Curves $V+ = 5V, V- = 0V, V_{CM} = 2.5V, R_L$ = Open **(Continued)**

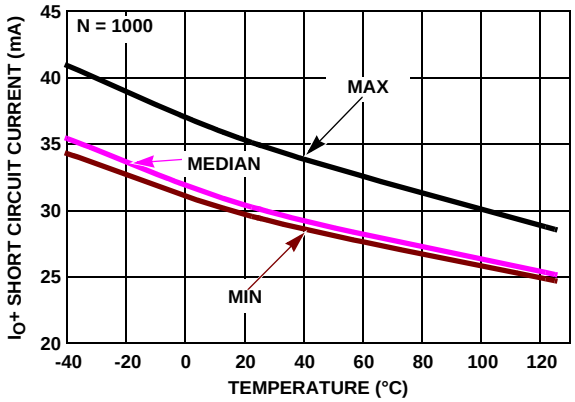


FIGURE 42. I_O+ SHORT CIRCUIT OUTPUT CURRENT vs TEMPERATURE V_{IN} = -2.55V, R_L = 10k, V_+, V_- = ±2.5V

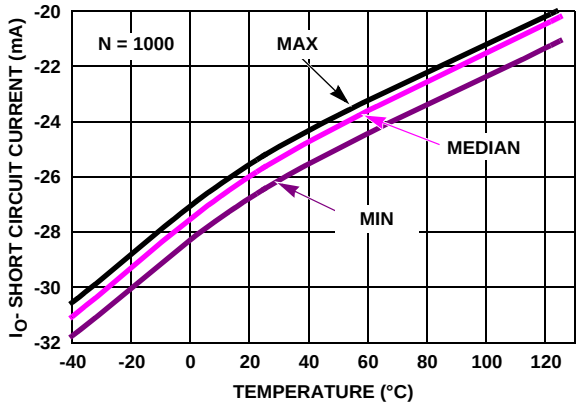
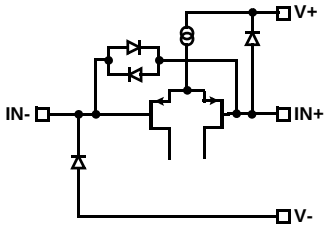
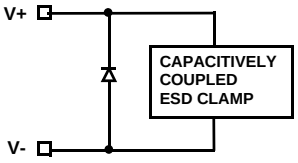
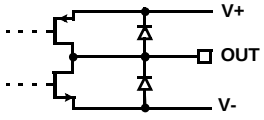
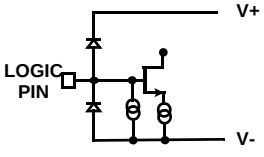


FIGURE 43. I_O- SHORT CIRCUIT OUTPUT CURRENT vs TEMPERATURE V_{IN} = +2.55V, R_L = 10k, V_+, V_- = ±2.5V

Pin Descriptions

ISL28158 (6 Ld SOT-23)	ISL28158 (8 Ld SOIC)	ISL28258 (8 Ld SOIC) (8 Ld MSOP)	PIN NAME	FUNCTION	EQUIVALENT CIRCUIT
	1, 5		NC	Not connected	
4	2	2 (A) 6 (B)	IN- IN- (A) IN- (B)	inverting input	 Circuit 1
3	3	3 (A) 5 (B)	IN+ IN+ (A) IN+ (B)	Non-inverting input	See Circuit 1
2	4	4	V-	Negative supply	 Circuit 2
1	6	1 (A) 7 (B)	OUT OUT (A) OUT (B)	Output	 Circuit 3
6	7	8	V+	Positive supply	See Circuit 2
5	8		$\overline{EN}$	Chip enable	 Circuit 3

Applications Information

Introduction

The ISL28158 is a single CMOS rail-to-rail input, output (RRIO) operational amplifier with an enable feature. The ISL28258 is a dual version without the enable feature. Both devices are designed to operate from single supply (2.4V to 5.5V) or dual supplies (±1.2V to ±2.75V).

Rail-to-Rail Input/Output

These devices feature PMOS inputs with an input common mode range that extends up to 0.3V beyond the V+ rail, and to 0.1V below the V- rail. The CMOS output features excellent drive capability, typically swinging to within 6mV of either rail with a 100kΩ load.

Results of Over-Driving the Output

Caution should be used when over-driving the output for long periods of time. Over-driving the output can occur in two ways. 1) the input voltage times the gain of the amplifier exceeds the supply voltage by a large value or, 2) The output current required is higher than the output stage can deliver. These conditions can result in a shift in the Input Offset Voltage (V_{OS}) as much as 1µV/hr. of exposure under these conditions.

IN+ and IN- Input Protection

All input terminals have internal ESD protection diodes to both positive and negative supply rails, limiting the input voltage to within one diode beyond the supply rails. They also contain back-to-back diodes across the input terminals (“Pin Descriptions” on page 11 - Circuit 1). For applications where the input differential voltage is expected to exceed 0.5V, an external series resistor must be used to ensure the input currents never exceed 5mA (Figure 44).

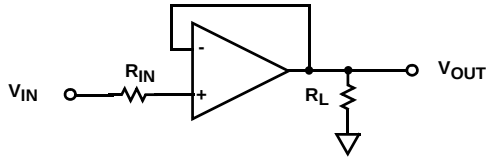


FIGURE 44. INPUT CURRENT LIMITING

Enable/Disable Feature

The ISL28158 offers an $\overline{EN}$ pin that disables the device when pulled up to at least 2.0V. In the disabled state (output in a high impedance state), the part consumes typically 10µA at room temperature. By disabling the part, multiple ISL28158 parts can be connected together as a MUX. In this configuration, the outputs are tied together in parallel and a channel can be selected by the $\overline{EN}$ pin. The loading effects of the feedback resistors of the disabled amplifier must be considered when multiple amplifier outputs are connected together. Note that feed through from the IN+ to IN- pins occurs on any Mux Amp disabled channel where the input differential voltage exceeds 0.5V (e.g., active channel V_{OUT} = 1V, while disabled channel V_{IN} = GND), so the mux implementation is best suited for small signal applications. If large signals are required, use series IN+ resistors, or large value R_F, to keep the feed through current low enough to minimize the impact on the active channel. See “Limitations of the Differential Input Protection” on page 12 for more details. The $\overline{EN}$ pin also has an internal pull down. If left open, the $\overline{EN}$ pin will pull to the negative rail and the device will be enabled by default. When not used, the $\overline{EN}$ pin should either be left floating or connected directly to the -V pin.

Limitations of the Differential Input Protection

If the input differential voltage is expected to exceed 0.5V, an external current limiting resistor must be used to ensure the input current never exceeds 5mA. For non inverting unity gain applications, the current limiting can be via a series IN+ resistor, or via a feedback resistor of appropriate value. For other gain configurations, the series IN+ resistor is the best choice, unless the feedback (R_F) and gain setting (R_G) resistors are both sufficiently large to limit the input current to 5mA.

Large differential input voltages can arise from several sources:

1) During open loop (comparator) operation. Used this way, the IN+ and IN- voltages don’t track, so differentials arise.

2) When the amplifier is disabled but an input signal is still present. An R_L or R_G to GND keeps the IN- at GND, while the varying IN+ signal creates a differential voltage. Mux Amp applications are similar, except that the active channel V_{OUT} determines the voltage on the IN- terminal.

3) When the slew rate of the input pulse is considerably faster than the op amp’s slew rate. If the V_{OUT} can’t keep up with the IN+ signal, a differential voltage results, and visible distortion occurs on the input and output signals. To avoid this issue, keep the input slew rate below 0.1V/µs, or use appropriate current limiting resistors.

Large (>2V) differential input voltages can also cause an increase in disabled I_{CC}.

Using Only One Channel

The ISL28258 is a dual op amp. If the application only requires one channel, the user must configure the unused channel to prevent it from oscillating. The unused channel will oscillate if the input and output pins are floating. This will result in higher than expected supply currents and possible noise injection into the channel being used. The proper way to prevent this oscillation is to short the output to the negative input and ground the positive input (as shown in Figure 45).

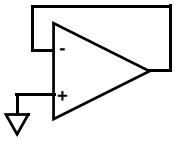


FIGURE 45. PREVENTING OSCILLATIONS IN UNUSED CHANNELS

Current Limiting

These devices have no internal current-limiting circuitry. If the output is shorted, it is possible to exceed the Absolute Maximum Rating for output current or power dissipation, potentially resulting in the destruction of the device.

Power Dissipation

It is possible to exceed the +125°C maximum junction temperatures under certain load and power-supply conditions. It is therefore important to calculate the maximum junction temperature (T_{JMAX}) for all applications to determine if power supply voltages, load conditions, or package type need to be modified to remain in the safe operating area. These parameters are related in Equation 1:

$$T_{JMAX} = T_{MAX} + (\theta_{JA} x PD_{MAXTOTAL}) \quad \text{(EQ. 1)}$$

where:

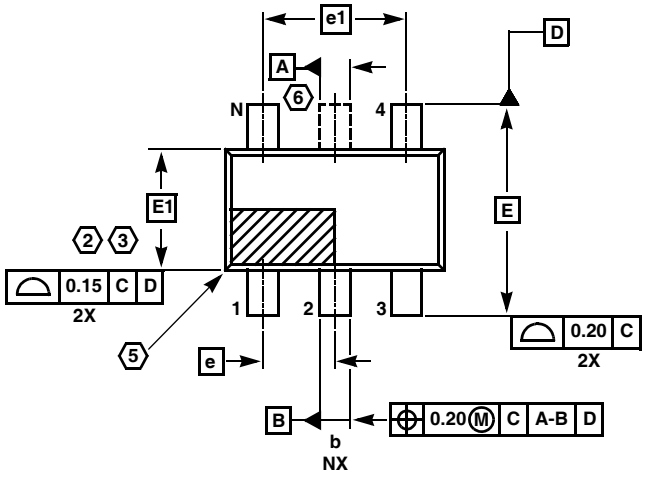
- $P_{DMAXTOTAL}$ is the sum of the maximum power dissipation of each amplifier in the package (PD_{MAX})
- PD_{MAX} for each amplifier can be calculated using Equation 2:

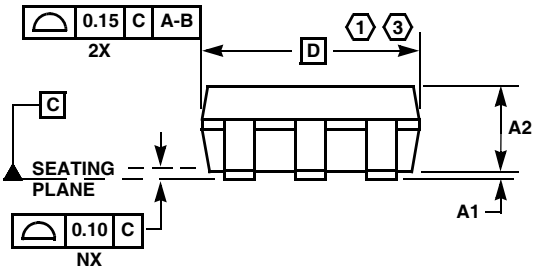
$$PD_{MAX} = 2*V_S \times I_{SMAX} + (V_S - V_{OUTMAX}) \times \frac{V_{OUTMAX}}{R_L} \quad \text{(EQ. 2)}$$

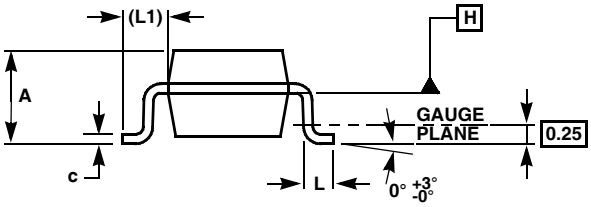
where:

- T_{MAX} = Maximum ambient temperature
- θ_{JA} = Thermal resistance of the package
- PD_{MAX} = Maximum power dissipation of 1 amplifier
- V_S = Supply voltage (Magnitude of V_+ and V_-)
- I_{MAX} = Maximum supply current of 1 amplifier
- V_{OUTMAX} = Maximum output voltage swing of the application
- R_L = Load resistance

SOT-23 Package Family







MDP0038

SOT-23 PACKAGE FAMILY

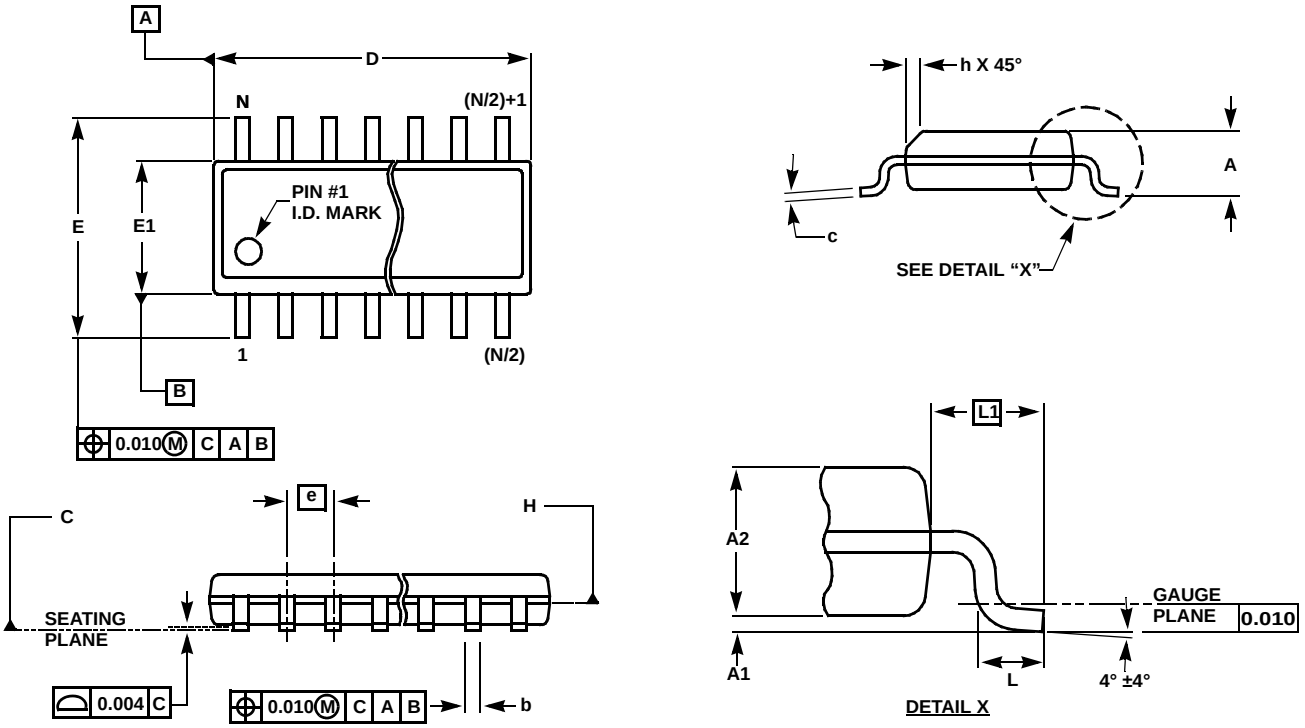
SYMBOL	MILLIMETERS		TOLERANCE
	SOT23-5	SOT23-6	
A	1.45	1.45	MAX
A1	0.10	0.10	±0.05
A2	1.14	1.14	±0.15
b	0.40	0.40	±0.05
c	0.14	0.14	±0.06
D	2.90	2.90	Basic
E	2.80	2.80	Basic
E1	1.60	1.60	Basic
e	0.95	0.95	Basic
e1	1.90	1.90	Basic
L	0.45	0.45	±0.10
L1	0.60	0.60	Reference
N	5	6	Reference

Rev. F 2/07

NOTES:

1. Plastic or metal protrusions of 0.25mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25mm maximum per side are not included.
3. This dimension is measured at Datum Plane “H”.
4. Dimensioning and tolerancing per ASME Y14.5M-1994.
5. Index area - Pin #1 I.D. will be located within the indicated zone (SOT23-6 only).
6. SOT23-5 version has no center lead (shown as a dashed line).

Small Outline Package Family (SO)



MDP0027

SMALL OUTLINE PACKAGE FAMILY (SO)

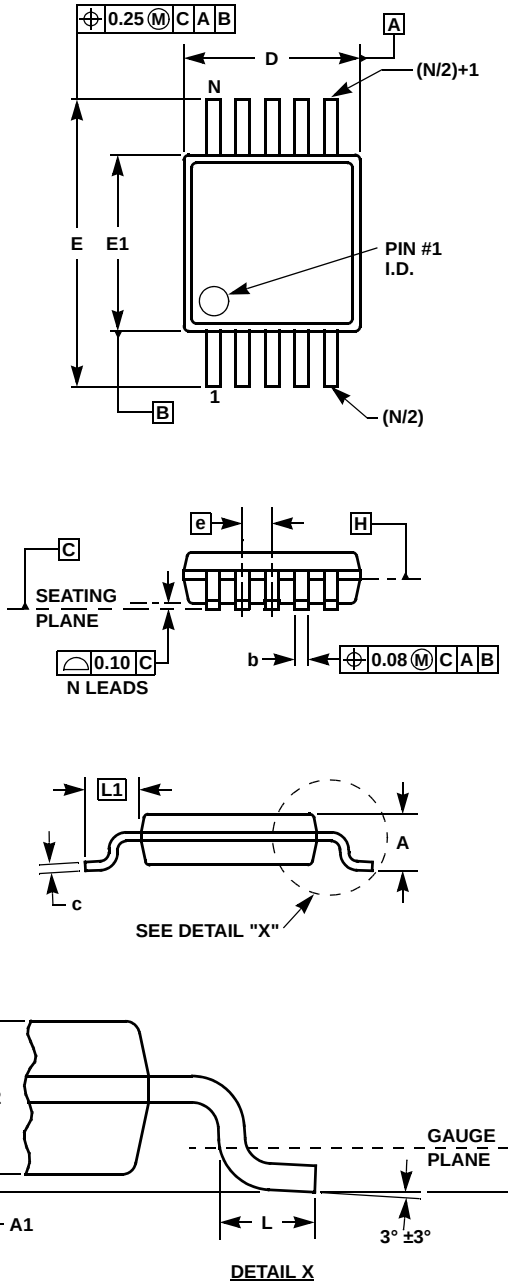
SYMBOL	INCHES							TOLERANCE	NOTES
	SO-8	SO-14	SO16 (0.150")	SO16 (0.300") (SOL-16)	SO20 (SOL-20)	SO24 (SOL-24)	SO28 (SOL-28)		
A	0.068	0.068	0.068	0.104	0.104	0.104	0.104	MAX	-
A1	0.006	0.006	0.006	0.007	0.007	0.007	0.007	±0.003	-
A2	0.057	0.057	0.057	0.092	0.092	0.092	0.092	±0.002	-
b	0.017	0.017	0.017	0.017	0.017	0.017	0.017	±0.003	-
c	0.009	0.009	0.009	0.011	0.011	0.011	0.011	±0.001	-
D	0.193	0.341	0.390	0.406	0.504	0.606	0.704	±0.004	1, 3
E	0.236	0.236	0.236	0.406	0.406	0.406	0.406	±0.008	-
E1	0.154	0.154	0.154	0.295	0.295	0.295	0.295	±0.004	2, 3
e	0.050	0.050	0.050	0.050	0.050	0.050	0.050	Basic	-
L	0.025	0.025	0.025	0.030	0.030	0.030	0.030	±0.009	-
L1	0.041	0.041	0.041	0.056	0.056	0.056	0.056	Basic	-
h	0.013	0.013	0.013	0.020	0.020	0.020	0.020	Reference	-
N	8	14	16	16	20	24	28	Reference	-

Rev. M 2/07

NOTES:

1. Plastic or metal protrusions of 0.006" maximum per side are not included.
2. Plastic interlead protrusions of 0.010" maximum per side are not included.
3. Dimensions "D" and "E1" are measured at Datum Plane "H".
4. Dimensioning and tolerancing per ASME Y14.5M-1994

Mini SO Package Family (MSOP)



MDP0043

MINI SO PACKAGE FAMILY

SYMBOL	MILLIMETERS		TOLERANCE	NOTES
	MSOP8	MSOP10		
A	1.10	1.10	Max.	-
A1	0.10	0.10	±0.05	-
A2	0.86	0.86	±0.09	-
b	0.33	0.23	+0.07/-0.08	-
c	0.18	0.18	±0.05	-
D	3.00	3.00	±0.10	1, 3
E	4.90	4.90	±0.15	-
E1	3.00	3.00	±0.10	2, 3
e	0.65	0.50	Basic	-
L	0.55	0.55	±0.15	-
L1	0.95	0.95	Basic	-
N	8	10	Reference	-

Rev. D 2/07

NOTES:

1. Plastic or metal protrusions of 0.15mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25mm maximum per side are not included.
3. Dimensions “D” and “E1” are measured at Datum Plane “H”.
4. Dimensioning and tolerancing per ASME Y14.5M-1994.