

N-Channel 100 V (D-S) 175 °C MOSFET

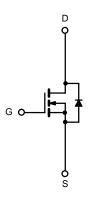
PRODUC	T SUMMARY	
V _{DS} (V)	R _{DS(on)} (Ω)	I _D (A)
100	0.004 at V _{GS} = 10 V	140 ^a

FEATURES

- TrenchFET[®] Power MOSFET
- New Package with Low Thermal Resistance
- 100 % R_g Tested







N-Channel MOSFET

ABSOLUTE MAXIMUM RATI	IGS T _C = 25 °C, unless oth	nerwise noted		
Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V _{DS}	100	V
Gate-Source Voltage		V _{GS}	± 20	v
Continuous Drain Current ($T_1 = 175 \text{ °C}$)	T _C = 25 °C	1	140 ^a	
$Continuous Drain Current (T_j = 175 C)$	T _C = 125 °C	- I _D	87 ^a	А
Pulsed Drain Current		I _{DM}	440	
Avalanche Current		I _{AR}	75	
Repetitive Avalanche Energy ^b	L = 0.1 mH	E _{AR}	280	mJ
Maximum Power Dissipation ^b	T _C = 25 °C	D	375 ^c	w
	T _A = 25 °C	– P _D –	3.75	VV V
Operating Junction and Storage Temperatu	re Range	T _J , T _{stg}	- 55 to 175	°C

THERMAL RESISTANCE RA	TINGS			
Parameter		Symbol	Limit	Unit
Junction-to-Ambient	PCB Mount (TO-263) ^d	R _{thJA}	40	°C/W
Junction-to-Case (Drain)		R _{thJC}	0.4	0/10

Notes:

a. Package limited.

a. Package infined.
b. Duty cycle ≤ 1 %.
c. See SOA curve for voltage derating.
d. When mounted on 1" square PCB (FR-4 material).

SPECIFICATIONS $T_J = 25 \circ$	C, unless o	therwise noted					
Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit	
Static							
Drain-Source Breakdown Voltage	V _{DS}	$V_{DS} = 0 V, I_{D} = 250 \mu A$	100			V	
Gate-Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}$, $I_D = 250 \ \mu A$	2		4	v	
Gate-Body Leakage	I _{GSS}	$V_{DS} = 0 V, V_{GS} = \pm 20 V$			± 100	nA	
		V _{DS} = 100 V, V _{GS} = 0 V			1		
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 100 V, V _{GS} = 0 V, T _J = 125 °C			50	μA	
		V _{DS} = 100 V, V _{GS} = 0 V, T _J = 175 °C			250		
On-State Drain Current ^a	I _{D(on)}	$V_{DS} \ge 5 \text{ V}, \text{ V}_{GS} = 10 \text{ V}$	120			А	
		V _{GS} = 10 V, I _D = 30 A		0.004			
Drain-Source On-State Resistance ^a	R _{DS(on)}	V _{GS} = 10 V, I _D = 30 A, T _J = 125 °C		0.017		Ω	
		V _{GS} = 10 V, I _D = 30 A, T _J = 175 °C		0.025			
Forward Transconductance ^a	9 _{fs}	V _{DS} = 15 V, I _D = 30 A	25			S	
Dynamic ^b	•	•					
Input Capacitance	C _{iss}			5500			
Output Capacitance	C _{oss}	V _{GS} = 0 V, V _{DS} = 25 V, f = 1 MHz		750		pF	
Reverse Transfer Capacitance	C _{rss}			280			
Total Gate Charge ^c	Qg			110	160		
Gate-Source Charge ^c	Q _{gs}	$V_{DS} = 50 \text{ V}, \text{ V}_{GS} = 10 \text{ V}, \text{ I}_{D} = 85 \text{ A}$		24		nC	
Gate-Drain Charge ^c	Q _{gd}			24			
Gate Resistance	R _g		1.0		6.2	Ω	
Turn-On Delay Time ^c	t _{d(on)}			20	30		
Rise Time ^c	t _r	$V_{DD} = 50 \text{ V}, \text{ R}_{1} = 0.6 \Omega$		125	200		
Turn-Off Delay Time ^c	t _{d(off)}	$I_D \cong 85 \text{ Å}, V_{GEN} = 10 \text{ V}, R_g = 2.5 \Omega$		55	85	ns	
Fall Time ^c	t _f			130	195	1	
Source-Drain Diode Ratings and Ch	aracteristics -	$\Gamma_{\rm C} = 25 \ {}^{\circ}{\rm C}^{\rm b}$		•			
Continuous Current	۱ _S				140	^	
Pulsed Current	I _{SM}				240	A	
Forward Voltage ^a	V _{SD}	I _F = 85 A, V _{GS} = 0 V		1.0	1.5	V	
Reverse Recovery Time	t _{rr}			70	140	ns	
Peak Reverse Recovery Charge	I _{RM(REC)}	I _F = 50 A, dl/dt = 100 A/μs		5.5	10	А	
Reverse Recovery Charge	Q _{rr}	1		0.19	0.35	μC	

Notes:

a. Pulse test; pulse width \leq 300 µs, duty cycle \leq 2 %.

b. Guaranteed by design, not subject to production testing.

c. Independent of operating temperature.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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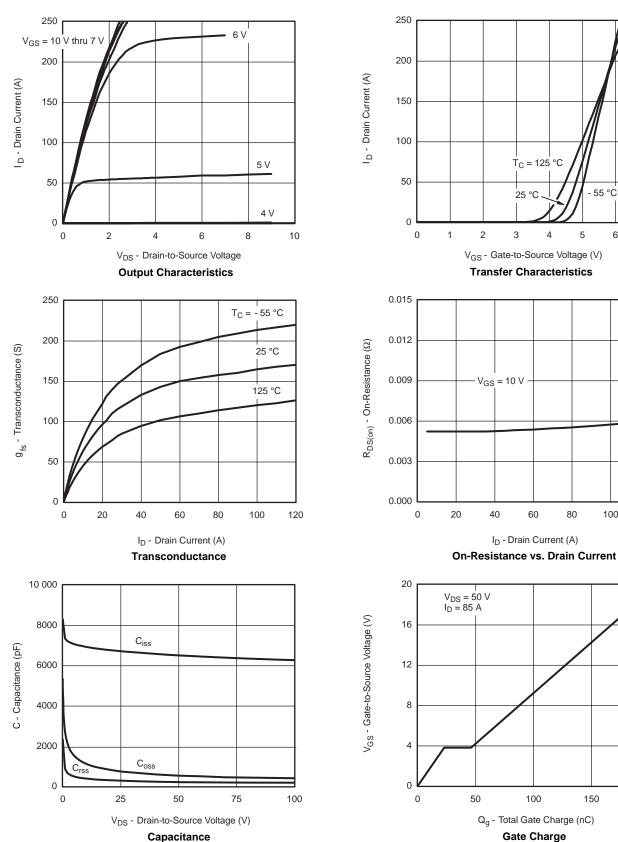


- 55 °C

T_C = 125 °C

Gate Charge

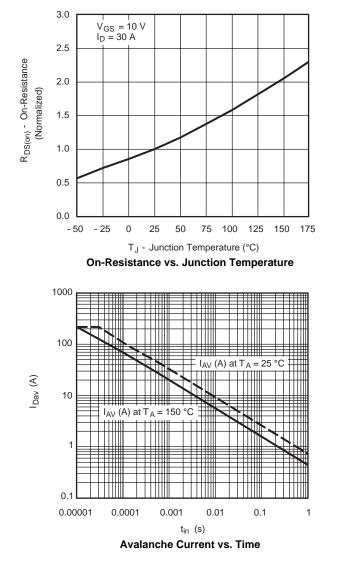
25 °C

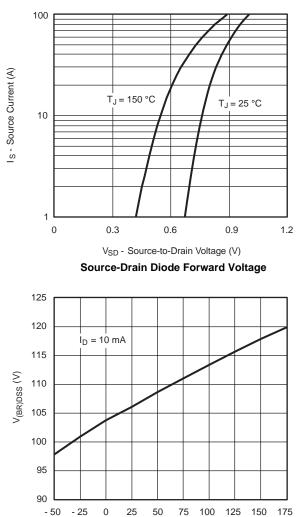


TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



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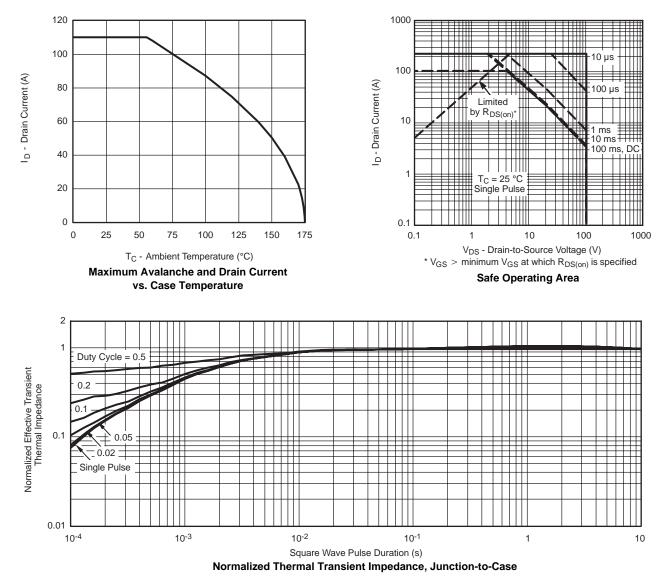


T_J - Junction Temperature (°C) Drain Source Breakdown vs. Junction Temperature

05CN10N TO263

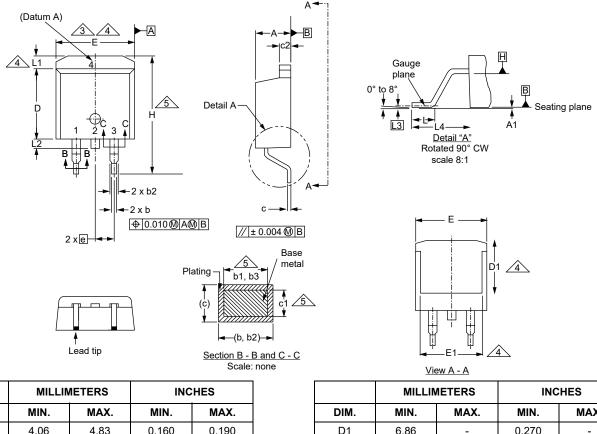


THERMAL RATINGS





TO-263AB (HIGH VOLTAGE)



DIM.	MIN.	MAX.	MIN.	MAX.
А	4.06	4.83	0.160	0.190
A1	0.00	0.25	0.000	0.010
b	0.51	0.99	0.020	0.039
b1	0.51	0.89	0.020	0.035
b2	1.14	1.78	0.045	0.070
b3	1.14	1.73	0.045	0.068
С	0.38	0.74	0.015	0.029
c1	0.38	0.58	0.015	0.023
c2	1.14	1.65	0.045	0.065
D	8.38	9.65	0.330	0.380
ECN: S-82 DWG: 5970	110-Rev. A, ′)	15-Sep-08		

Notes

1. Dimensioning and tolerancing per ASME Y14.5M-2018.

2. Dimensions are shown in millimeters (inches).

3. Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005") per side. These dimensions are measured at the outmost extremes of the plastic body at datum A.

4. Thermal PAD contour optional within dimension E, L1, D1 and E1.

5. Dimension b1 and c1 apply to base metal only.

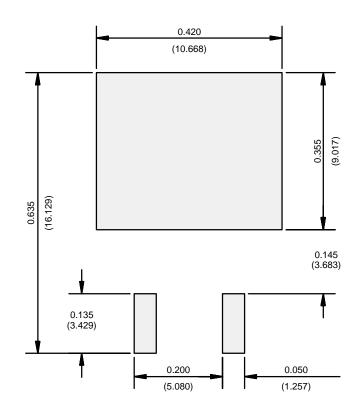
6. Datum A and B to be determined at datum plane H.

7. Outline conforms to JEDEC outline to TO-263AB.

05CN10N TO263



RECOMMENDED MINIMUM PADS FOR D²PAK: 3-Lead



Recommended Minimum Pads Dimensions in Inches/(mm)



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