JSMICRO SEMICONDUCTOR

BT151-500R

1. Product profile

1.1 General description

Planar passivated SCR (Silicon Controlled Rectifier) in a SOT78 plastic package.

1.2 Features and benefits

- High reliability
- High surge current capability
- High thermal cycling performance

1.3 Applications

- Ignition circuits
- Motor control
- Protection Circuits
- Static switching

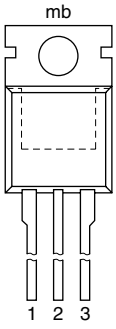
1.4 Quick reference data

Table 1. Quick reference

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DRM}	repetitive peak off-state voltage		-	-	500	V
$I_{T(AV)}$	average on-state current	half sine wave; $T_{mb} \leq 109$ °C; see Figure 3	-	-	7.5	A
$I_{T(RMS)}$	RMS on-state current	half sine wave; $T_{mb} \leq 109$ °C; see Figure 1; see Figure 2	-	-	12	A
Static characteristics						
I_{GT}	gate trigger current	V_D = 12 V; T_j = 25 °C; I_T = 100 mA; see Figure 8	-	2	15	mA

2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	K	cathode		
2	A	anode		
3	G	gate		
mb	mb	anode		

SOT78
(TO-220AB; SC-46)

3. Ordering information

Table 3. Ordering information

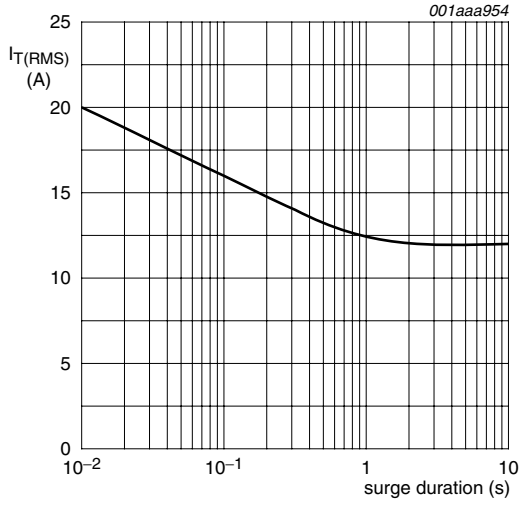
Type number	Package		
	Name	Description	Version
BT151-500R	TO-220AB; SC-46	plastic single-ended package; heatsink mounted; 1 mounting hole; 3-lead TO-220AB	SOT78

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DRM}	repetitive peak off-state voltage		-	500	V
V_{RRM}	repetitive peak reverse voltage		-	500	V
$I_{T(AV)}$	average on-state current	half sine wave; $T_{mb} \leq 109$ °C; see Figure 3	-	7.5	A
$I_{T(RMS)}$	RMS on-state current	half sine wave; $T_{mb} \leq 109$ °C; see Figure 1; see Figure 2	-	12	A
dI_T/dt	rate of rise of on-state current	I_T = 20 A; I_G = 50 mA; dI_G/dt = 50 mA/µs	-	50	A/µs
I_{GM}	peak gate current		-	2	A
P_{GM}	peak gate power		-	5	W
T_{stg}	storage temperature		-40	150	°C
T_j	junction temperature		-	125	°C
I_{TSM}	non-repetitive peak on-state current	half sine wave; t_p = 8.3 ms; $T_{j(init)}$ = 25 °C	-	132	A
		half sine wave; t_p = 10 ms; $T_{j(init)}$ = 25 °C; see Figure 4; see Figure 5	-	120	A
I^2t	I2t for fusing	t_p = 10 ms; sine-wave pulse	-	72	A^2s
$P_{G(AV)}$	average gate power	over any 20 ms period	-	0.5	W
V_{RGM}	peak reverse gate voltage		-	5	V



$f = 50Hz; T_{mb} = 109\,°C$

Fig 1. RMS on-state current as a function of surge duration; maximum values

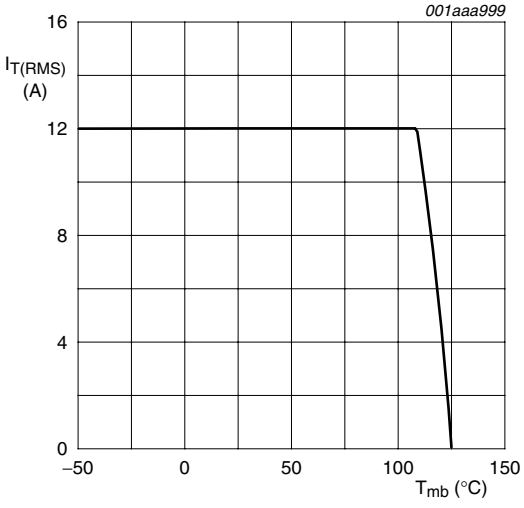
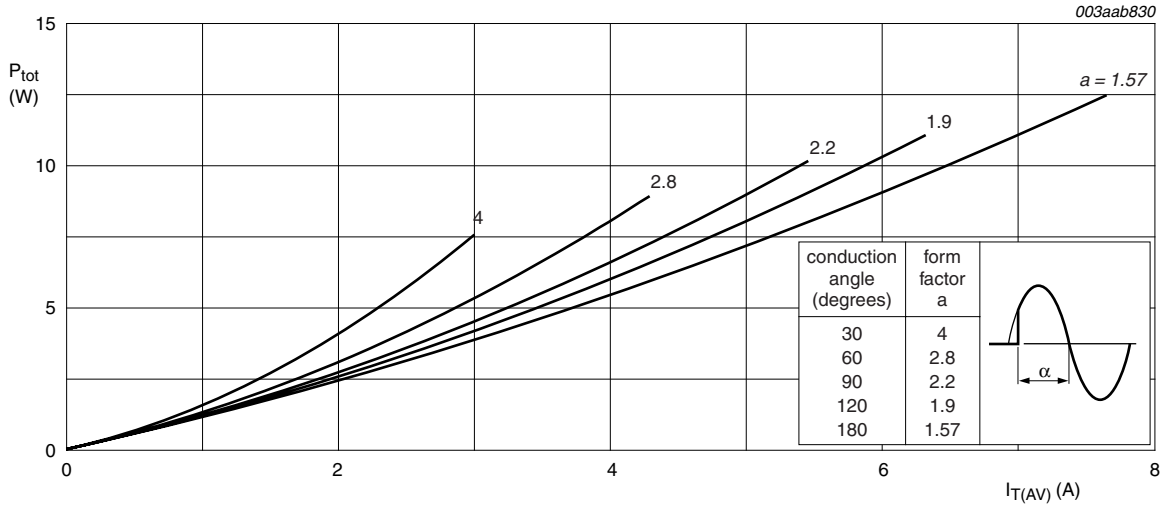
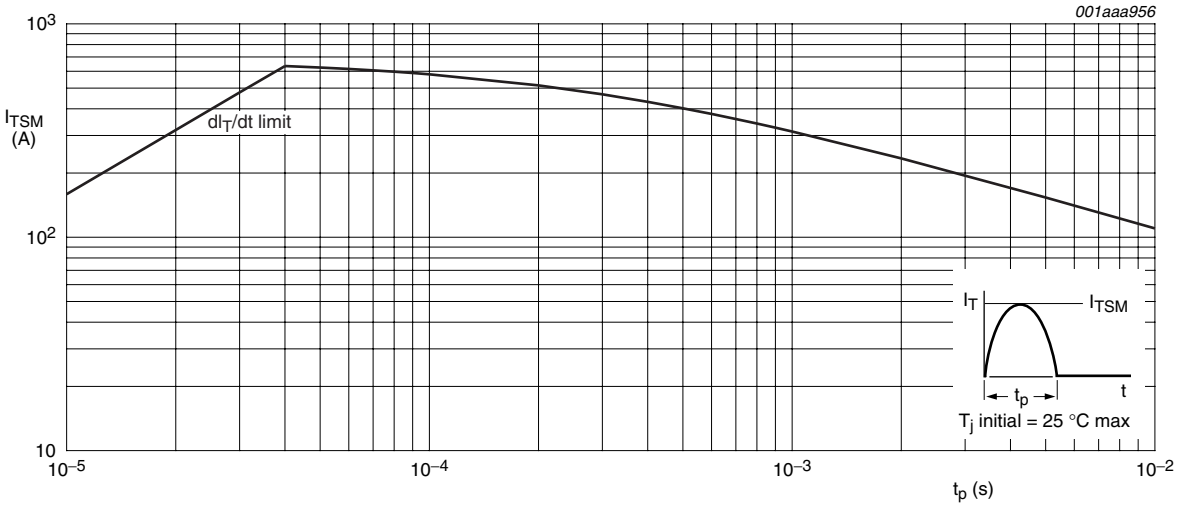


Fig 2. RMS on-state current as a function of mounting base temperature; maximum values



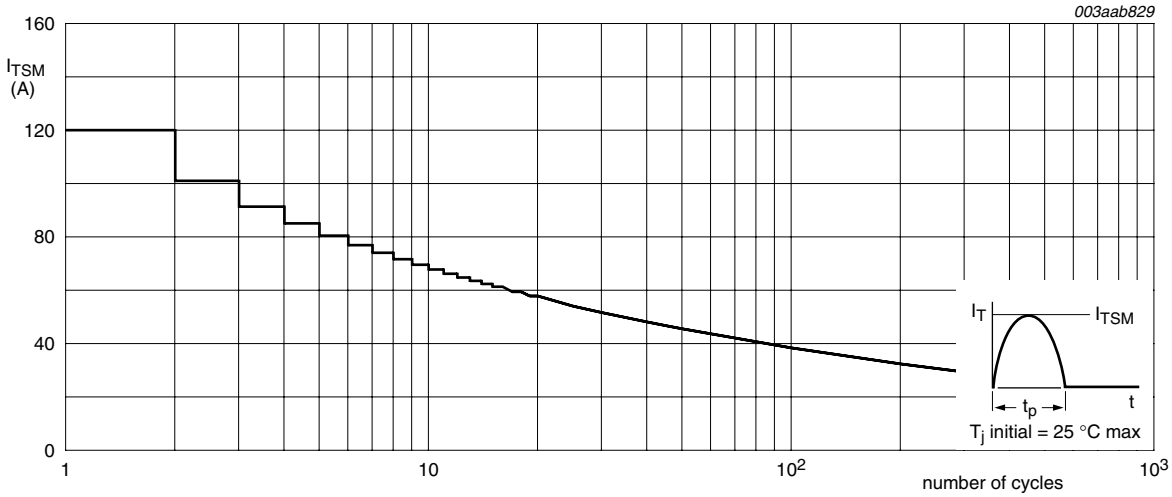
$$a = \text{form factor} = I_{T(RMS)} / I_{T(AV)}$$

Fig 3. Total power dissipation as a function of average on-state current; maximum values



$$t_p = 10\,ms$$

Fig 4. Non-repetitive peak on-state current as a function of pulse width for sinusoidal currents; maximum values



$f = 50Hz$

Fig 5. Non-repetitive peak on-state current as a function of the number of sinusoidal current cycles; maximum values

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j\text{-}mb)}$	thermal resistance from junction to mounting base	see Figure 6	-	-	1.3	K/W
$R_{th(j\text{-}a)}$	thermal resistance from junction to ambient free air		-	60	-	K/W

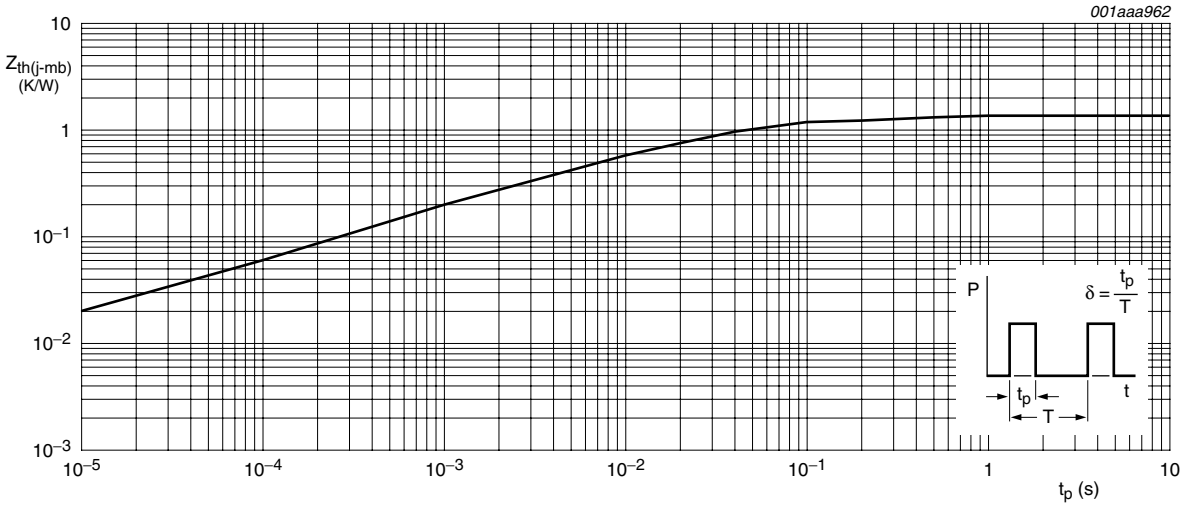
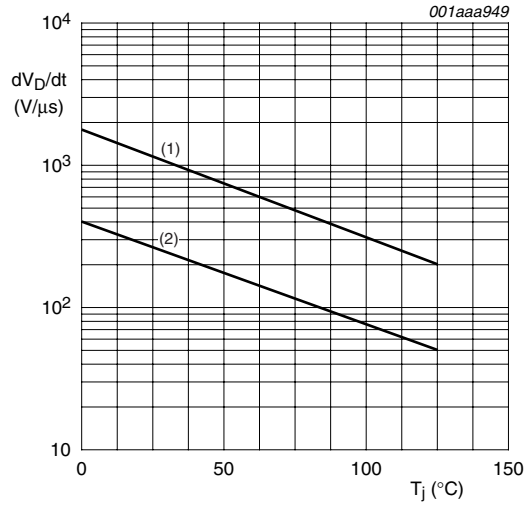


Fig 6. Transient thermal impedance from junction to mounting base as a function of pulse width

6. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
I_{GT}	gate trigger current	V_D = 12 V; T_j = 25 °C; I_T = 100 mA; see Figure 8	-	2	15	mA
I_L	latching current	V_D = 12 V; T_j = 25 °C; see Figure 9	-	10	40	mA
I_H	holding current	V_D = 12 V; T_j = 25 °C; see Figure 10	-	7	20	mA
V_T	on-state voltage	I_T = 23 A; T_j = 25 °C; see Figure 11	-	1.4	1.75	V
V_{GT}	gate trigger voltage	I_T = 100 mA; V_D = 12 V; T_j = 25 °C; see Figure 12	-	0.6	1.5	V
		I_T = 100 mA; V_D = 500 V; T_j = 125 °C	0.25	0.4	-	V
I_D	off-state current	V_D = 500 V; T_j = 125 °C	-	0.1	0.5	mA
I_R	reverse current	V_R = 500 V; T_j = 125 °C	-	0.1	0.5	mA
Dynamic characteristics						
dV_D/dt	rate of rise of off-state voltage	V_{DM} = 335 V; T_j = 125 °C; exponential waveform; gate open circuit	50	130	-	V/µs
		V_{DM} = 335 V; T_j = 125 °C; R_{GK} = 100 Ω; exponential waveform; see Figure 7	200	1000	-	V/µs
t_{gt}	gate-controlled turn-on time	I_{TM} = 40 A; V_D = 500 V; I_G = 100 mA; dI_G/dt = 5 A/µs; T_j = 25 °C	-	2	-	µs
t_q	commutated turn-off time	V_{DM} = 335 V; T_j = 125 °C; I_{TM} = 20 A; V_R = 25 V; $(dI_T/dt)_M$ = 30 A/µs; dV_D/dt = 50 V/µs; R_{GK} = 100 Ω	-	70	-	µs



(1) $R_{GK} = 100\ \Omega$
(2) Gate open circuit

Fig 7. Critical rate of rise of off-state voltage as a function of junction temperature; minimum values

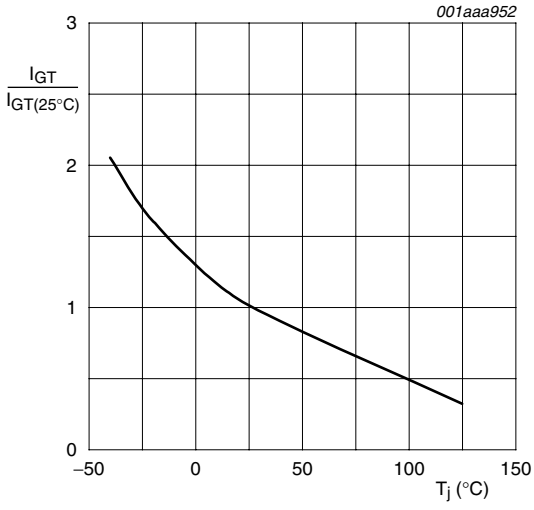


Fig 8. Normalized gate trigger current as a function of junction temperature

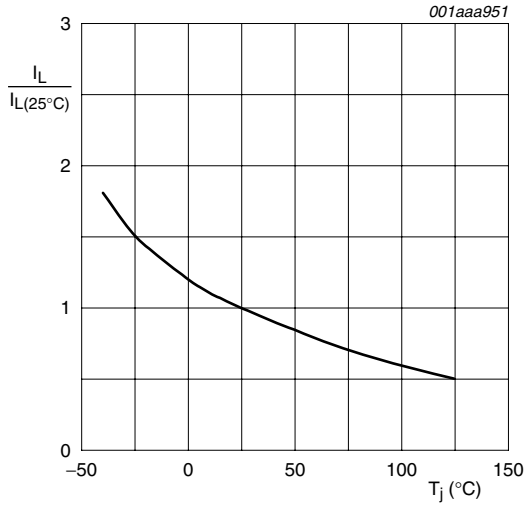


Fig 9. Normalized latching current as a function of junction temperature

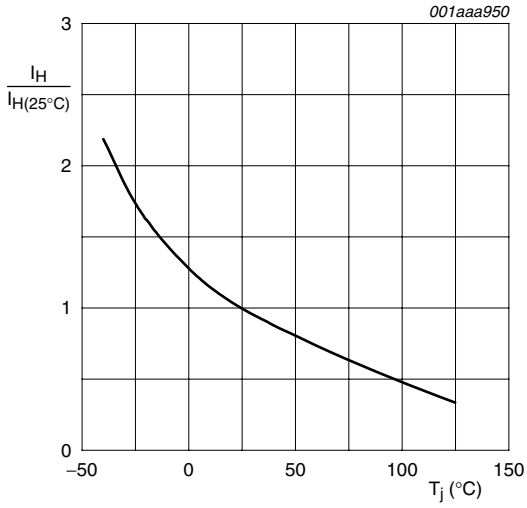
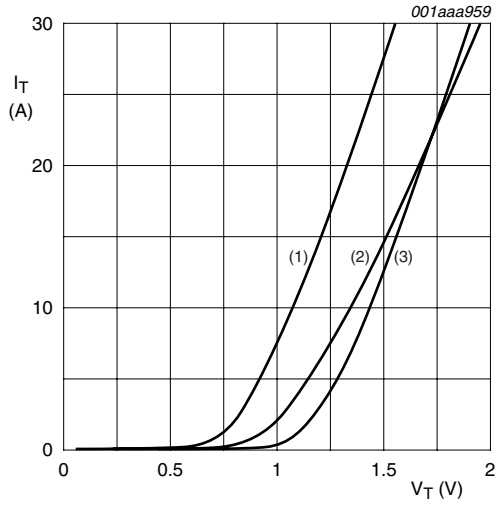


Fig 10. Normalized holding current as a function of junction temperature



$V_0 = 1.06\ V$; $R_s = 0.0304\ \Omega$
(1) $T_j = 150\ °C$; typical values
(2) $T_j = 150\ °C$; maximum values
(3) $T_j = 25\ °C$; maximum values

Fig 11. On-state current as a function of on-state voltage

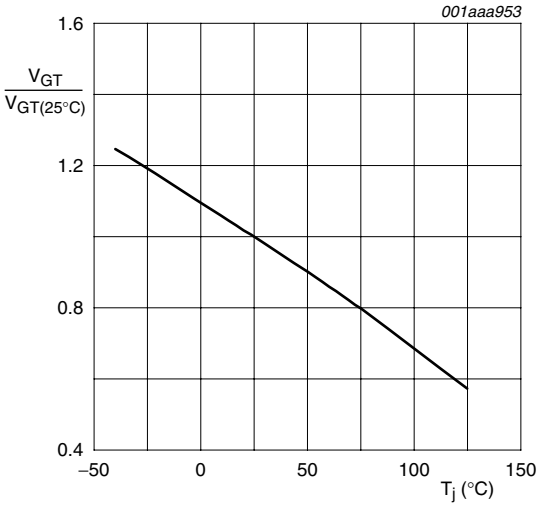
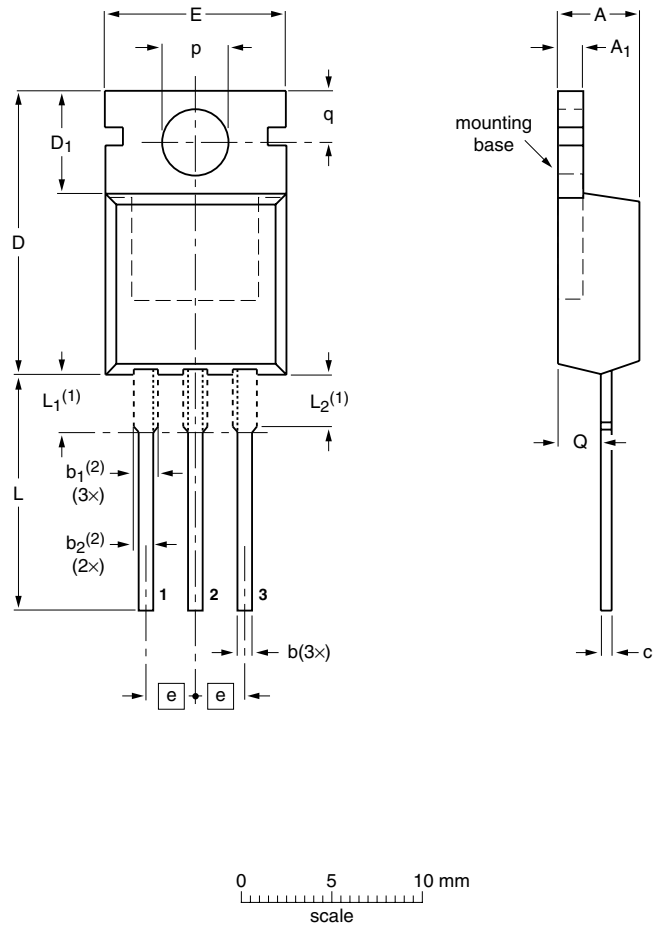


Fig 12. Normalized gate trigger voltage as a function of junction temperature

7. Package outline

Plastic single-ended package; heatsink mounted; 1 mounting hole; 3-lead TO-220AB **SOT78**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1	b	b_1(2)	b_2(2)	c	D	D_1	E	e	L	L_1(1)	L_2(1) max.	p	q	Q
mm	4.7 4.1	1.40 1.25	0.9 0.6	1.6 1.0	1.3 1.0	0.7 0.4	16.0 15.2	6.6 5.9	10.3 9.7	2.54	15.0 12.8	3.30 2.79	3.0	3.8 3.5	3.0 2.7	2.6 2.2

Notes

1. Lead shoulder designs may vary.
2. Dimension includes excess dambar.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT78		3-lead TO-220AB	SC-46			~~08-04-23~~ 08-06-13

Fig 13. Package outline SOT78 (TO-220AB)