JSMICRO SEMICONDUCTOR

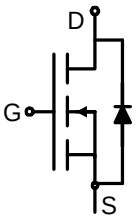
JSM50N06D

Product Summary

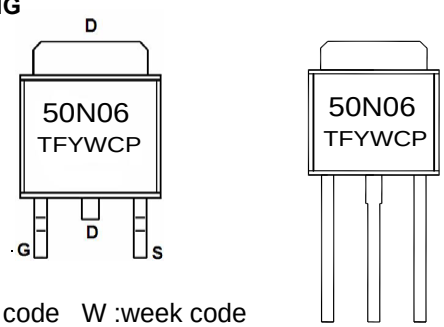
V_{DS}	60	V
$R_{DS(on),max}$ SMDversion	15	mΩ
I_D	50	A

TO-252 **TO-251**

Equivalent Circuit



MARKING



Y :year code W :week code

Features

- For fast switching converters and sync. rectification
- N-channel enhancement - normal level
- 175 °C operating temperature
- Avalanche rated
- Pb-free lead plating, RoHS compliant

Typical Applications

- Power Supplies
- Converters
- Power Motor Controls
- Bridge Circuits

Maximum ratings, at T_j=25 °C, unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current	I_D	T_C =25 °C[1)]	50	A
Pulsed drain current	$I_{D,pulse}$	T_C=25 °C[2)]	400	
Avalanche energy, single pulse	E_{AS}	I_D=50 A, R_{GS}=25 Ω	810	mJ
Reverse diode dv/dt	dv/dt	I_D=50 A, V_{DS}=48 V, di/dt=100 A/µs, $T_{j,max}$=175 °C	6	kV/µs
Gate source voltage	V_{GS}		±20	V
Power dissipation	P_{tot}	T_C=25 °C	300	W
Operating and storage temperature	T_j, T_{stg}		-55 ... 175	°C
IEC climatic category; DIN IEC 68-1			55/175/56	

[1)] Current is limited by bondwire; with an R_{thJC}=0.5 the chip is able to carry 160A

[2)] See figure 3

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Thermal characteristics						
Thermal resistance, junction - case	R_{thJC}		-	-	0.5	K/W
SMD version, device on PCB	R_{thJA}	minimal footprint	-	-	62	
		6 cm^2 cooling area[3)]	-	-	40	
Electrical characteristics, at T_j=25 °C, unless otherwise specified						
Static characteristics						
Drain-source breakdown voltage	$V_{(BR)DSS}$	V_{GS}=0 V, I_D=250uA	60	-	-	V
Gate threshold voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=250 µA	2.1	3	4	
Zero gate voltage drain current	I_{DSS}	V^j_{DS}=48 V, V_{GS}=0 V, T =25 °C	-	0.01	1	µA
Gate-source leakage current	I_{GSS}	V_{GS}=±20 V, V_{DS}=0 V	-		±50	nA
Drain-source on-state resistance	$R_{DS(on)}$	V_{GS}=10 V, I_D=30 A			15	mΩ
Gate resistance	R_G		-	1.9	-	Ω
Transconductance	g_{fs}	$\|V_{DS}\|>2\|I_D\|R_{DS(on)max}$, I_D=50 A	74	148	-	S

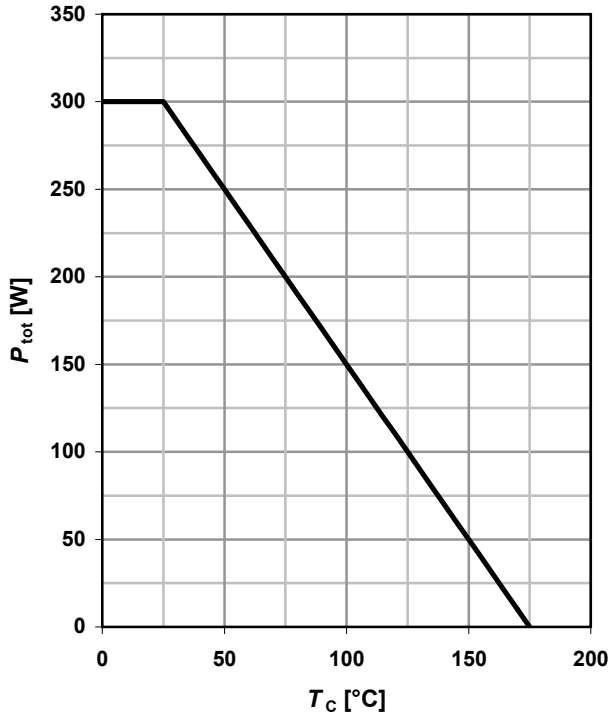
[3)] Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm^2 (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Dynamic characteristics						
Input capacitance	C_{iss}	V_{GS}=0 V, V_{DS}=30 V, f=1 MHz	-	4600	6100	pF
Output capacitance	C_{oss}		-	1500	2000	
Reverse transfer capacitance	C_{rss}		-	350	525	
Turn-on delay time	$t_{d(on)}$	V_{DD}=30 V, V_{GS}=10 V, I_D=30 A, R_G=2.2 Ω	-	21	32	ns
Rise time	t_r		-	31	47	
Turn-off delay time	$t_{d(off)}$		-	59	88	
Fall time	t_f		-	30	45	
Gate Charge Characteristics[4)]						
Gate to source charge	Q_{gs}	V_{DD}=30 V, I_D=50 A, V_{GS}=0 to 10 V	-	24	32	nC
Gate charge at threshold	$Q_{g(th)}$		-	9.7	13	
Gate to drain charge	Q_{gd}		-	51	76	
Switching charge	Q_{sw}		-	65	95	
Gate charge total	Q_g		-	126	167	
Gate plateau voltage	$V_{plateau}$		-	5.2	-	V
Output charge	Q_{oss}	V_{DD}=30 V, V_{GS}=0 V	-	47	62	
Reverse Diode						
Diode continous forward current	I_S	T_C=25 °C	-	-	100	A
Diode pulse current	$I_{S,pulse}$		-	-	400	
Diode forward voltage	V_{SD}	V_{GS}=0 V, I_F=30 A, T_j=25 °C	-	0.93	1.3	V
Reverse recovery time	t_{rr}	V_R=30 V, I_F=I_S, di_F/dt=30 A/µs	-	60	75	ns
Reverse recovery charge	Q_{rr}		-	130	160	nC

[4)] See figure 16 for gate charge parameter definition

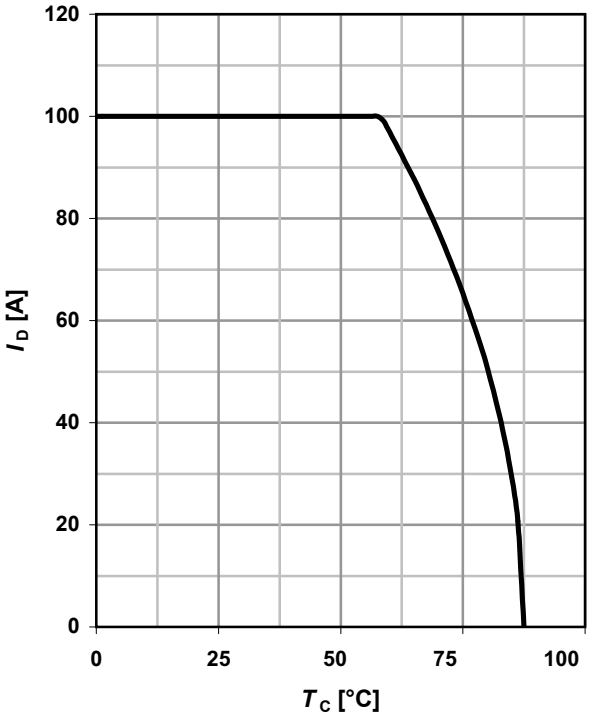
1 Power dissipation

P_{tot}=f(T_C); V_{GS}≥6 V



2 Drain current

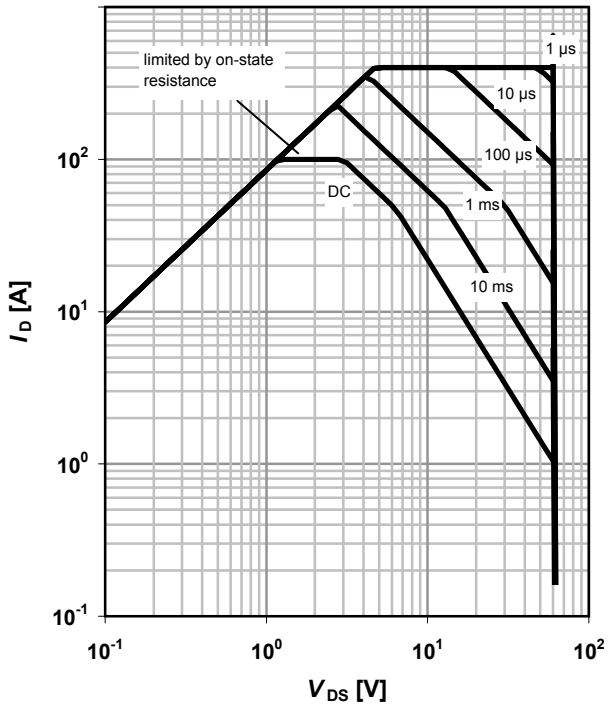
I_D=f(T_C); V_{GS}≥10 V



3 Safe operating area

I_D=f(V_{DS}); T_C=25 °C; D=0

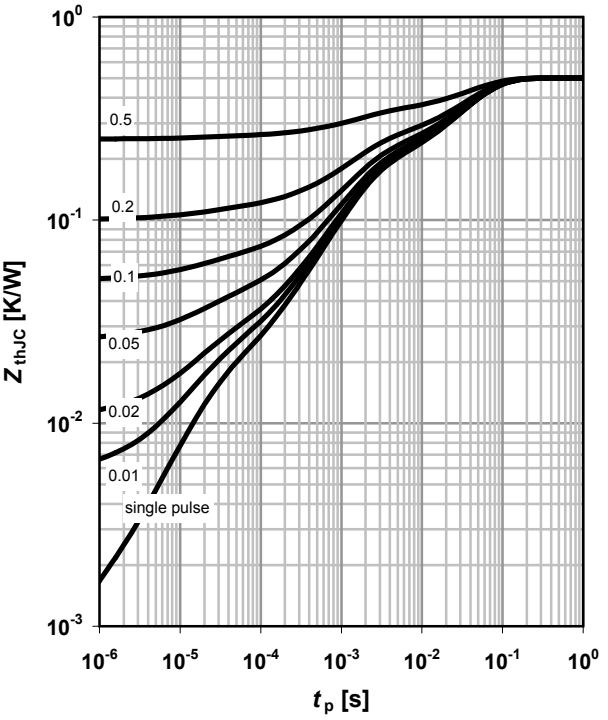
parameter: t_p



4 Max. transient thermal impedance

Z_{thJC}=f(t_p)

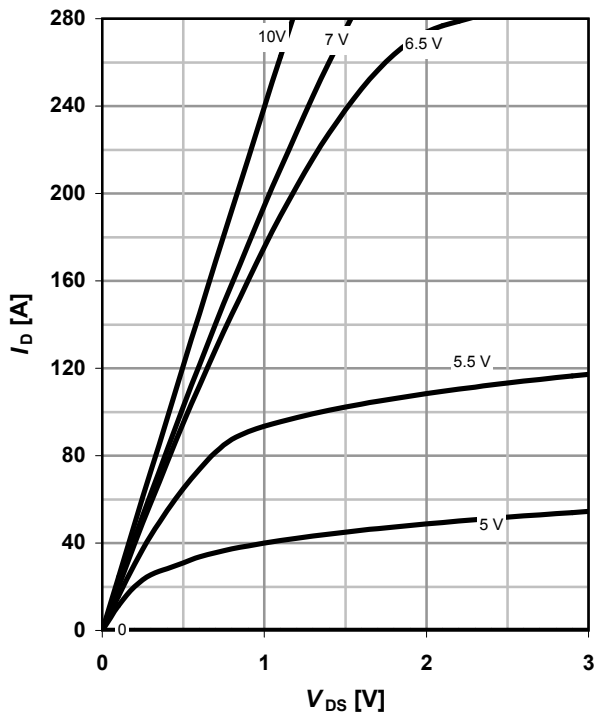
parameter: D=t_p/T



5 Typ. output characteristics

I_D=f(V_{DS}); T_j=25 °C

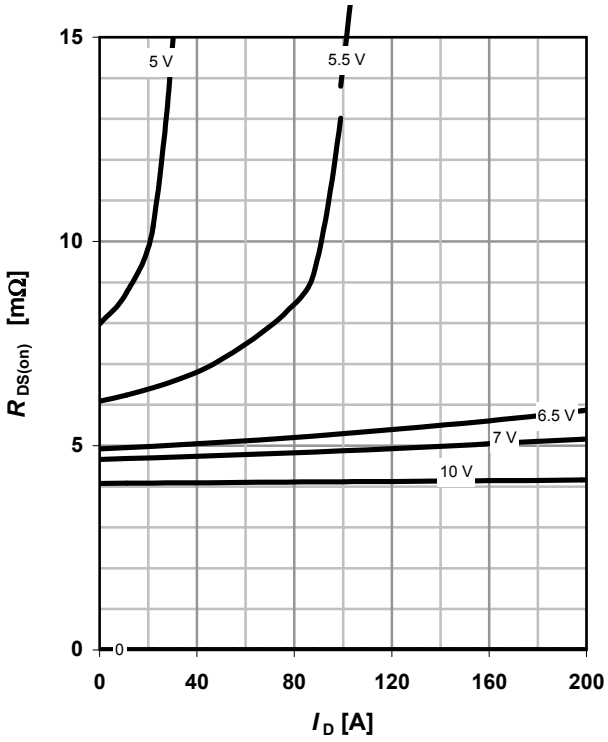
parameter: V_{GS}



6 Typ. drain-source on resistance

$R_{DS(on)}$=f(I_D); T_j=25 °C

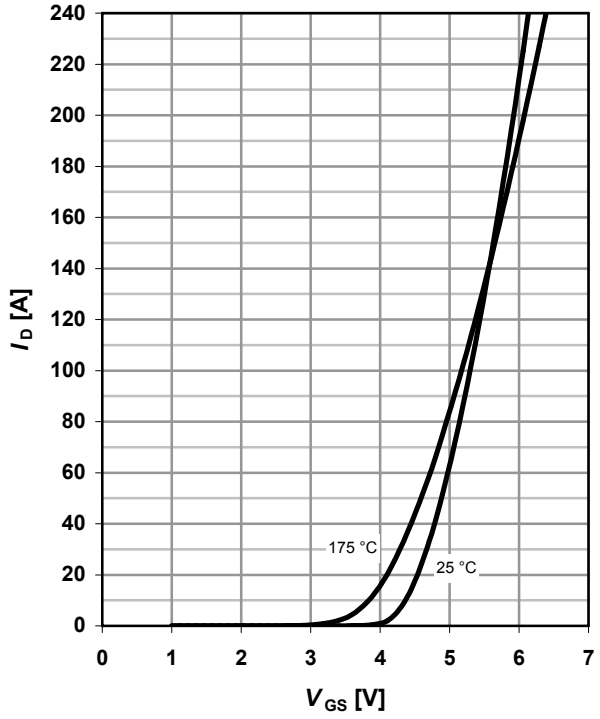
parameter: V_{GS}



7 Typ. transfer characteristics

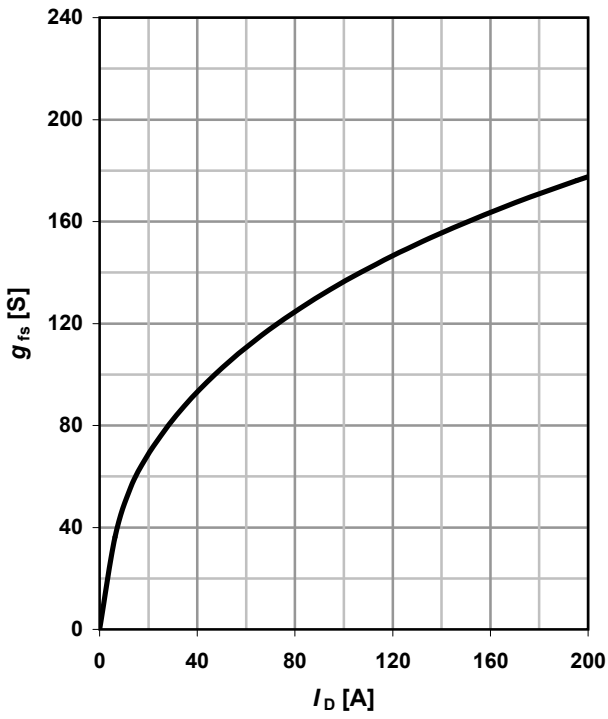
I_D=f(V_{GS}); $|V_{DS}|>2|I_D|R_{DS(on)max}$

parameter: T_j



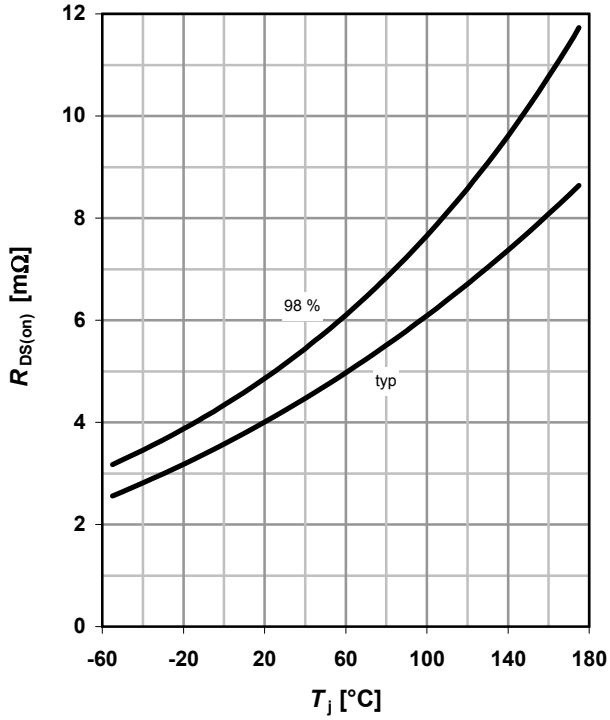
8 Typ. forward transconductance

g_{fs}=f(I_D); T_j=25 °C



9 Drain-source on-state resistance

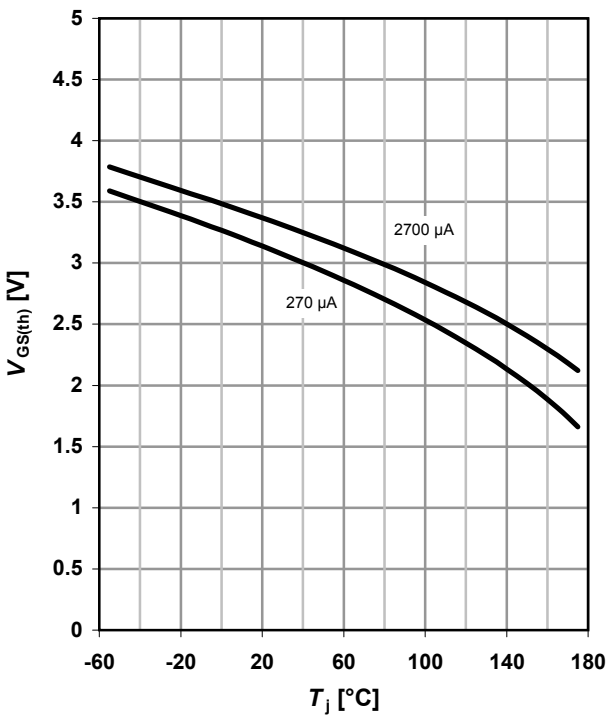
$R_{DS(on)}=f(T_j)$; $I_D=30$ A; $V_{GS}=10$ V



10 Typ. gate threshold voltage

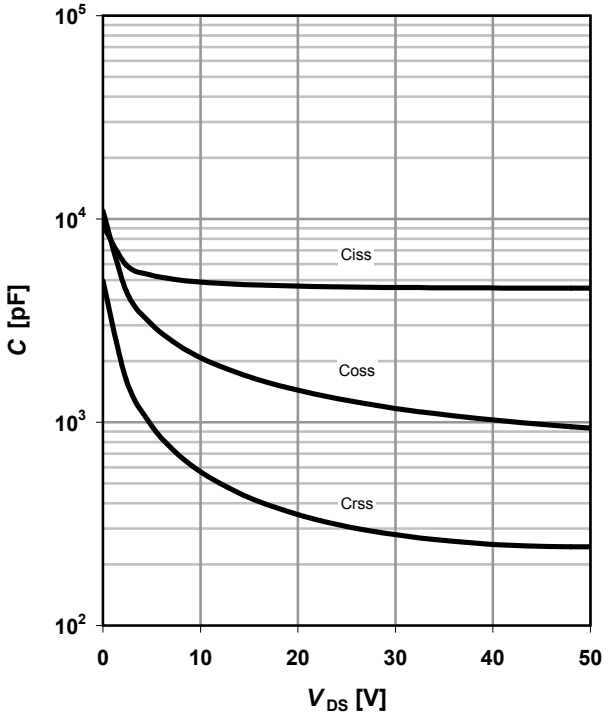
$V_{GS(th)}=f(T_j)$ $V_{GS}=V_{DS}$

parameter: I_D



11 Typ. capacitances

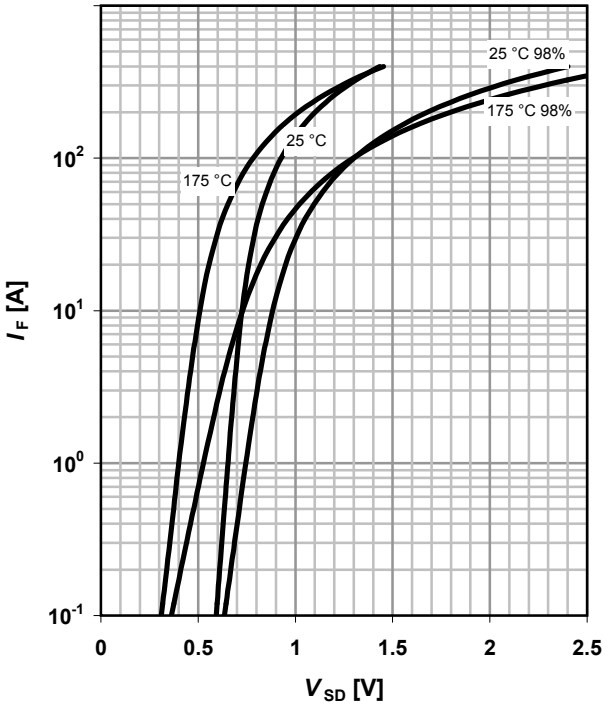
$C=f(V_{DS})$; $V_{GS}=0$ V; $f=1$ MHz



12 Forward characteristics of reverse diode

$I_F=f(V_{SD})$

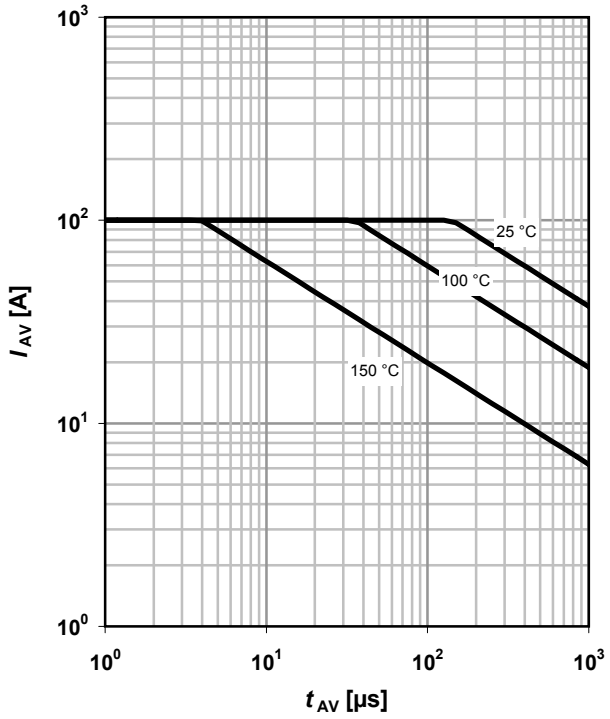
parameter: T_j



13 Avalanche characteristics

I_{AS}=f(t_{AV}); R_{GS}=25 Ω

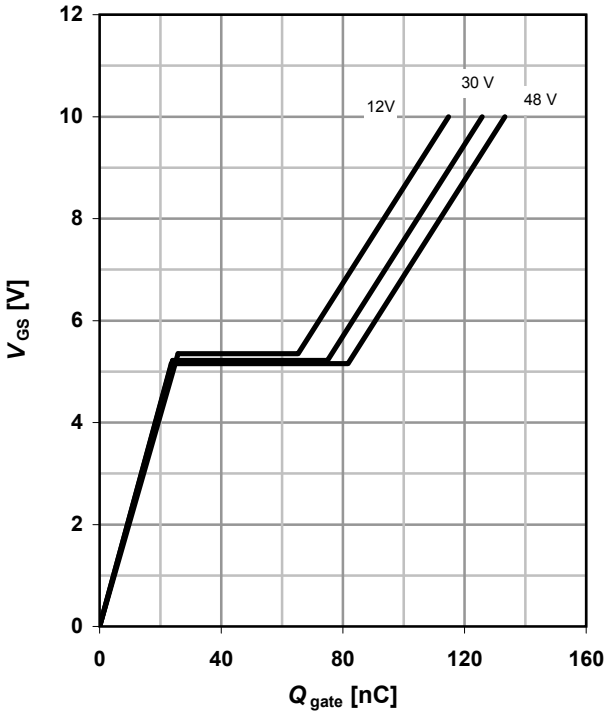
parameter: $T_{j(start)}$



14 Typ. gate charge

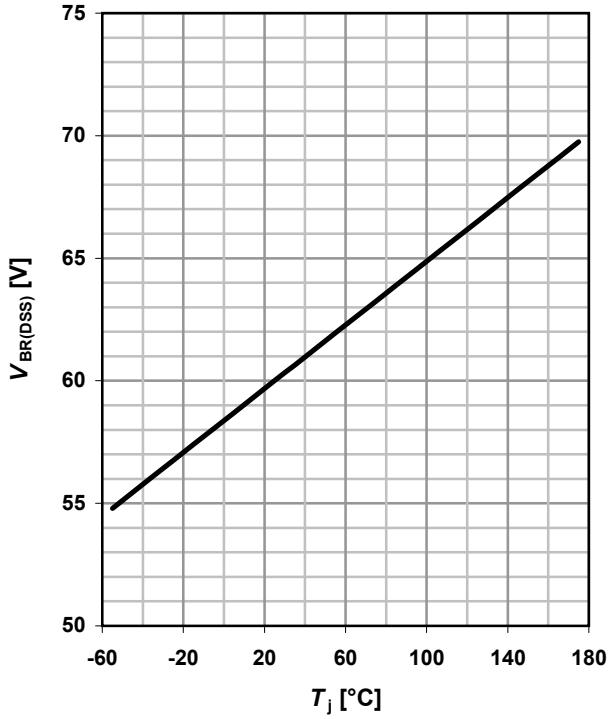
V_{GS}=f(Q_{gate}); I_D=30 A pulsed

parameter: V_{DD}

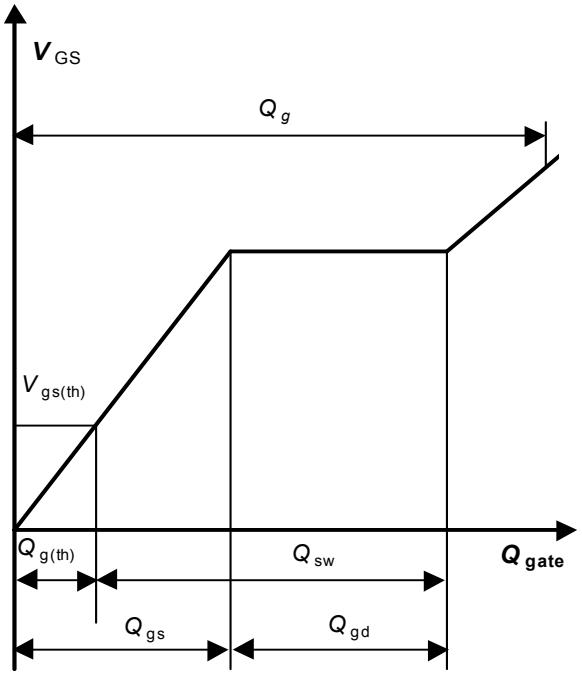


15 Drain-source breakdown voltage

$V_{BR(DSS)}$=f(T_j); I_D=1 mA

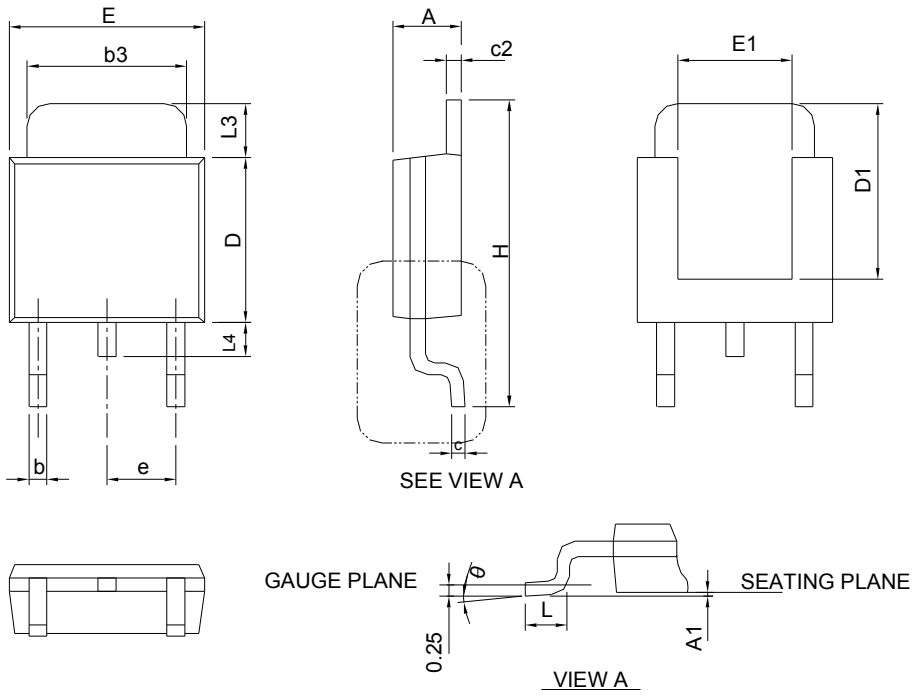


16 Gate charge waveforms



Package Information

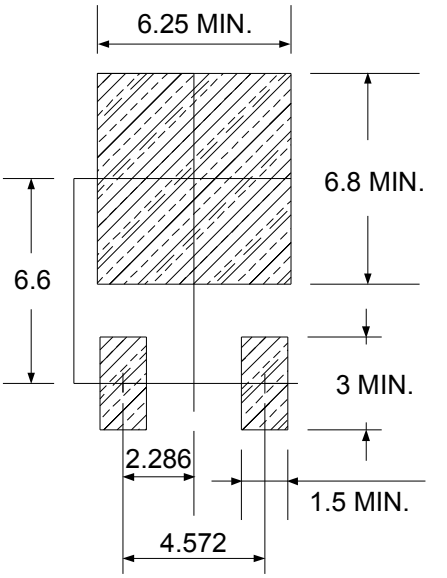
TO-252



SYMBOL	TO-252			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	2.18	2.39	0.086	0.094
A1		0.13		0.005
b	0.50	0.89	0.020	0.035
b3	4.95	5.46	0.195	0.215
c	0.46	0.61	0.018	0.024
c2	0.46	0.89	0.018	0.035
D	5.33	6.22	0.210	0.245
D1	4.57	6.00	0.180	0.236
E	6.35	6.73	0.250	0.265
E1	3.81	6.00	0.150	0.236
e	2.29 BSC		0.090 BSC	
H	9.40	10.41	0.370	0.410
L	0.90	1.78	0.035	0.070
L3	0.89	2.03	0.035	0.080
L4		1.02		0.040
θ	0°	8°	0°	8°

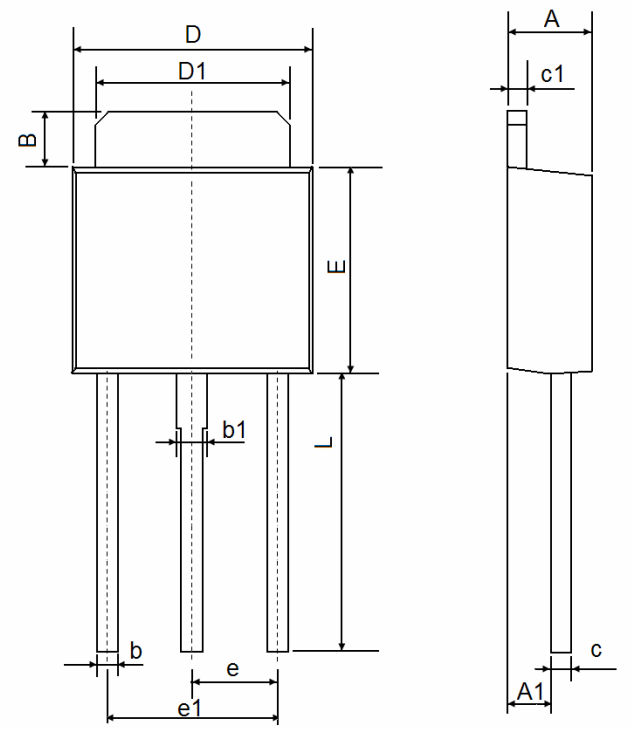
Note : Follow JEDEC TO-252 .

RECOMMENDED LAND PATTERN



UNIT: mm

TO-251 Package Information



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	2.200	2.400	0.087	0.094
A1	1.050	1.350	0.042	0.054
B	0.700	1.000	0.028	0.040
b	0.500	0.700	0.020	0.028
b1	0.700	0.900	0.028	0.035
c	0.430	0.580	0.017	0.023
c1	0.430	0.580	0.017	0.023
D	6.350	6.650	0.250	0.262
D1	5.200	5.400	0.205	0.213
E	5.400	6.000	0.213	0.237
e	2.300 TYP.		0.091 TYP.	
e1	4.500	4.700	0.177	0.185
L	4.900	9.400	0.194	0.372

Notes

1. All dimensions are in millimeters.
2. Tolerance ±0.10mm (4 mil) unless otherwise specified
3. Package body sizes exclude mold flash and gate burrs. Mold flash at the non-lead sides should be less than 5 mils.
4. Dimension L is measured in gauge plane.
5. Controlling dimension is millimeter, converted inch dimensions are not necessarily exac