NCE N-Channel Super Trench Power MOSFET

Description

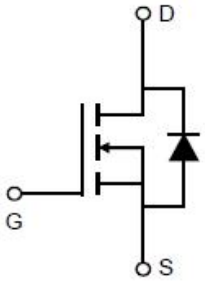
The NCEP30T17GU uses **Super Trench** technology that is uniquely optimized to provide the most efficient high frequency switching performance. Both conduction and switching power losses are minimized due to an extremely low combination of $R_{DS(ON)}$ and Q_g. This device is ideal for high-frequency switching and synchronous rectification.

General Features

- V_{DS} =30V,I_D =170A
  $R_{DS(ON)}$=0.97mΩ (typical) @ V_{GS}=10V
  $R_{DS(ON)}$=1.25mΩ (typical) @ V_{GS}=4.5V
- Excellent gate charge x $R_{DS(on)}$ product(FOM)
- Very low on-resistance $R_{DS(on)}$
- 150 °C operating temperature
- Pb-free lead plating
- 100% UIS tested

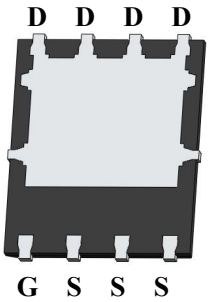
Application

- DC/DC Converter
- Ideal for high-frequency switching and synchronous rectification



Schematic Diagram

Top View



Bottom View

100% UIS TESTED!

100% ΔVds TESTED!

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
P30T17GU	NCEP30T17GU	DFN5X6-8L	-	-	-

Absolute Maximum Ratings (T_C=25℃unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	30	V
Gate-Source Voltage	V_{GS}	±20	V
Drain Current-Continuous **(Silicon Limited)**	I_D	170	A
Drain Current-Continuous(T_C=100℃)	I_D (100℃)	125	A
Pulsed Drain Current	I_{DM}	680	A
Maximum Power Dissipation	P_D	135	W
Derating factor		1.08	W/℃
Single pulse avalanche energy (Note 1)	E_{AS}	1350	mJ
Operating Junction and Storage Temperature Range	T_J,T_{STG}	-55 To 150	℃

Thermal Characteristic

Thermal Resistance,Junction-to-Case	$R_{\theta JC}$	0.926	℃/W

Electrical Characteristics (T_C=25℃unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V I_D=250μA	30		-	V
Zero Gate Voltage Drain Current	I_{DSS} T_J=25℃	V_{DS}=30V,V_{GS}=0V	-	-	1	μA
	I_{DSS} T_J=55℃		-	-	1.5	μA
Gate-Body Leakage Current	I_{GSS}	V_{GS}=±5V,V_{DS}=0V	-	-	±80	nA
		V_{GS}=±20V,V_{DS}=0V	-	-	±100	nA
On Characteristics						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=250μA	1.0	1.5	2.0	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	V_{GS}=10V, I_D=20A	0.75	0.97	1.2	mΩ
		V_{GS}=4.5V, I_D=20A	1	1.25	1.5	mΩ
Forward Transconductance	g_{FS}	V_{DS}=5V,I_D=20A		80	-	S
Dynamic Characteristics						
Input Capacitance	C_{lss}	V_{DS}=15V,V_{GS}=0V, F=1.0MHz	-	5300	6890	PF
Output Capacitance	C_{oss}		-	1800	2600	PF
Reverse Transfer Capacitance	C_{rss}		-	100	200	PF
Switching Characteristics						
Turn-on Delay Time(Note 2)	$t_{d(on)}$	V_{DD}=15V,I_D=20A V_{GS}=10V,R_G=1.6Ω	-	12	-	nS
Turn-on Rise Time(Note 2)	t_r		-	6.5	-	nS
Turn-Off Delay Time(Note 2)	$t_{d(off)}$		-	48	-	nS
Turn-Off Fall Time(Note 2)	t_f		-	7.5	-	nS
Total Gate Charge	Q_g	V_{DS}=15V,I_D=20A, V_{GS}=10V	-	90	126	nC
Gate-Source Charge	Q_{gs}		-	12	18	nC
Gate-Drain Charge	Q_{gd}		-	13	19.5	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage	V_{SD}	V_{GS}=0V,I_S=20A	-	-	1.2	V
Diode Forward Current	I_S		-	-	170	A
Reverse Recovery Time	t_{rr}	T_J = 25°C, I_F = I_S di/dt = 100A/μs	-	-	30	nS
Reverse Recovery Charge	Qrr		-	-	110	nC

Notes:

1. E_{AS} condition : Tj=25℃,V_{DD}=20V,V_G=10V,L=0.5mH,Rg=25Ω
2. Guaranteed by design, not subject to production
3. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsin k, assuming a maximum junction temperature of TJ(MAX)=150° C. The SOA curve provides a single pulse rating.

Typical Electrical and Thermal Characteristics

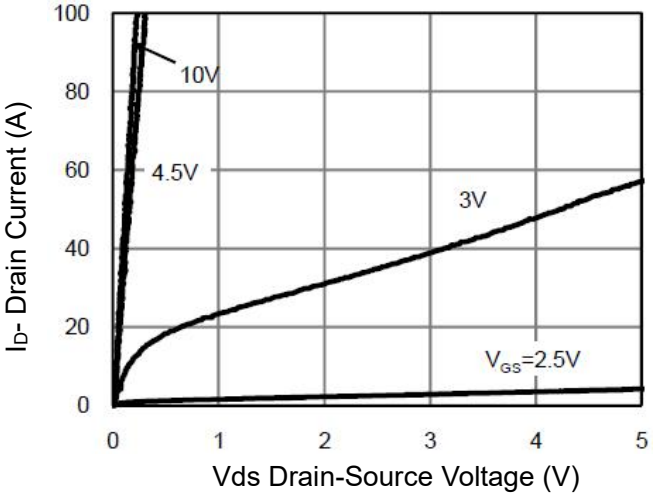


Figure 1 Output Characteristics

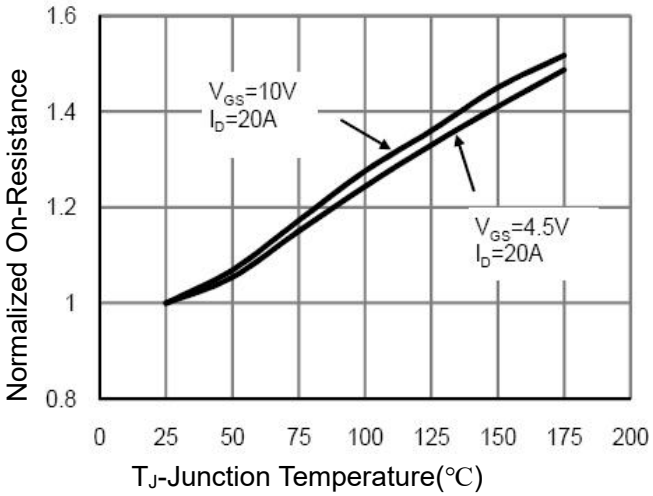


Figure 4 Rdson-Junction Temperature

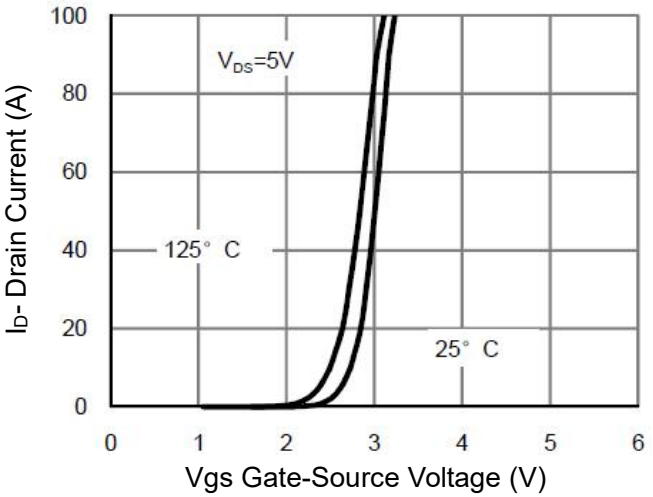


Figure 2 Transfer Characteristics

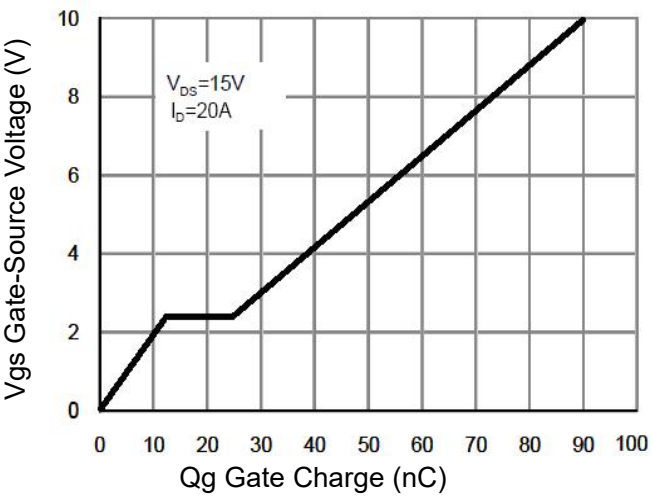


Figure 5 Gate Charge

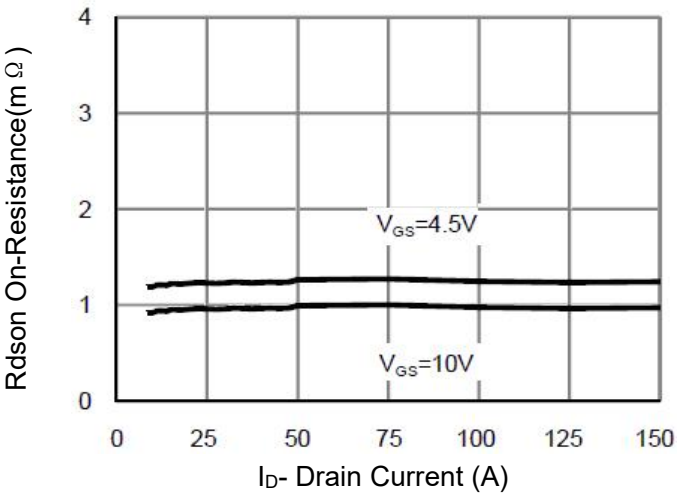


Figure 3 Rdson- Drain Current

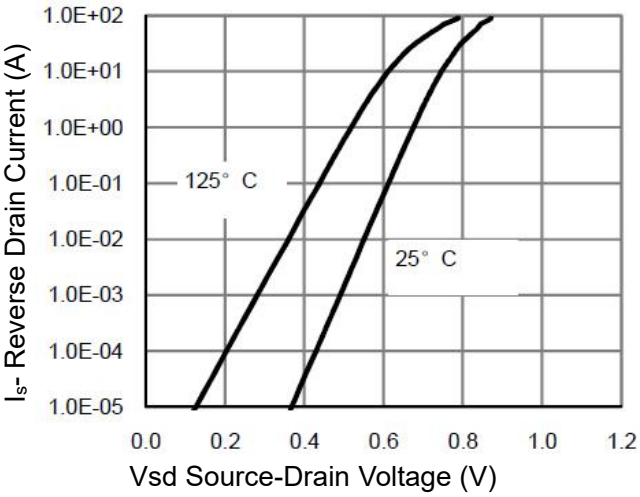


Figure 6 Source- Drain Diode Forward

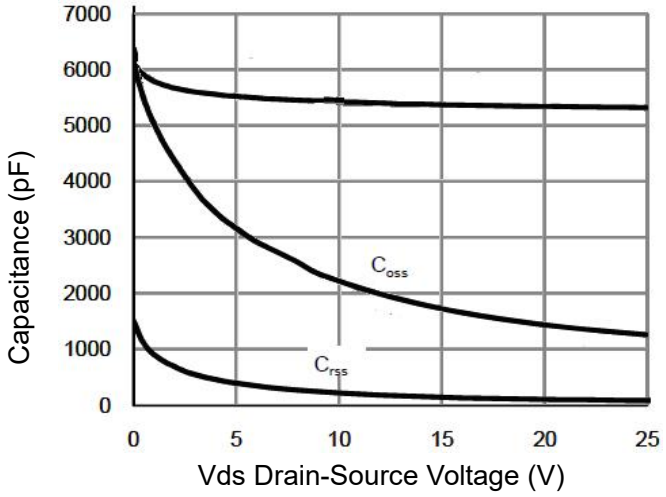


Figure 7 Capacitance vs Vds

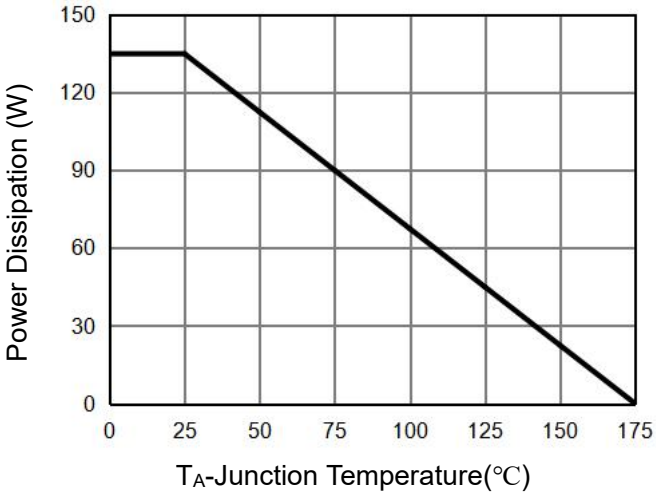


Figure 9 Power De-rating

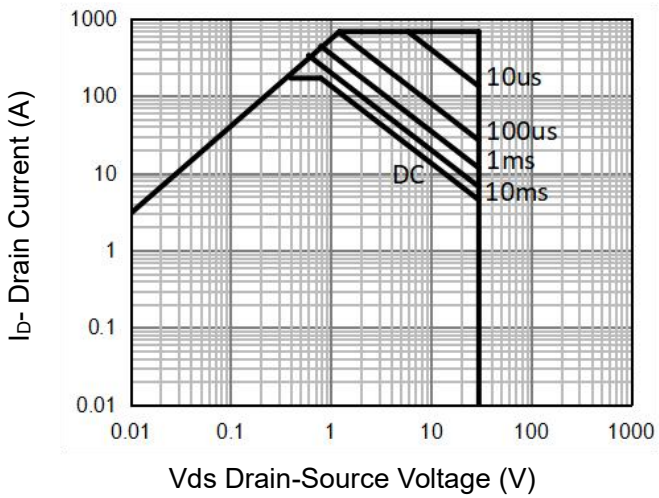


Figure 8 Safe Operation Area (Note3)

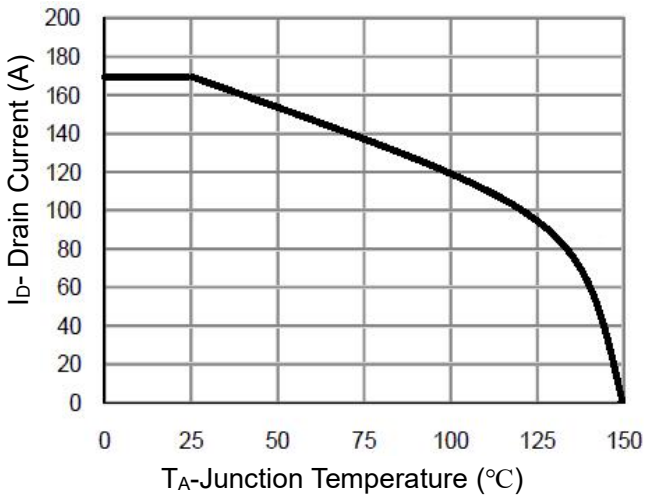


Figure 10 Current De-rating

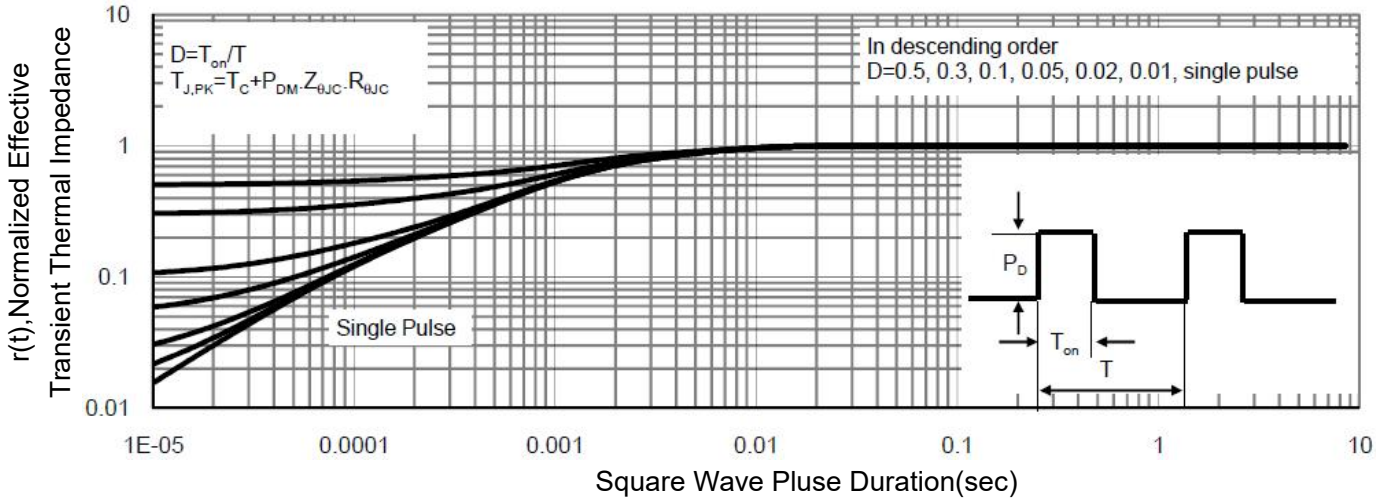
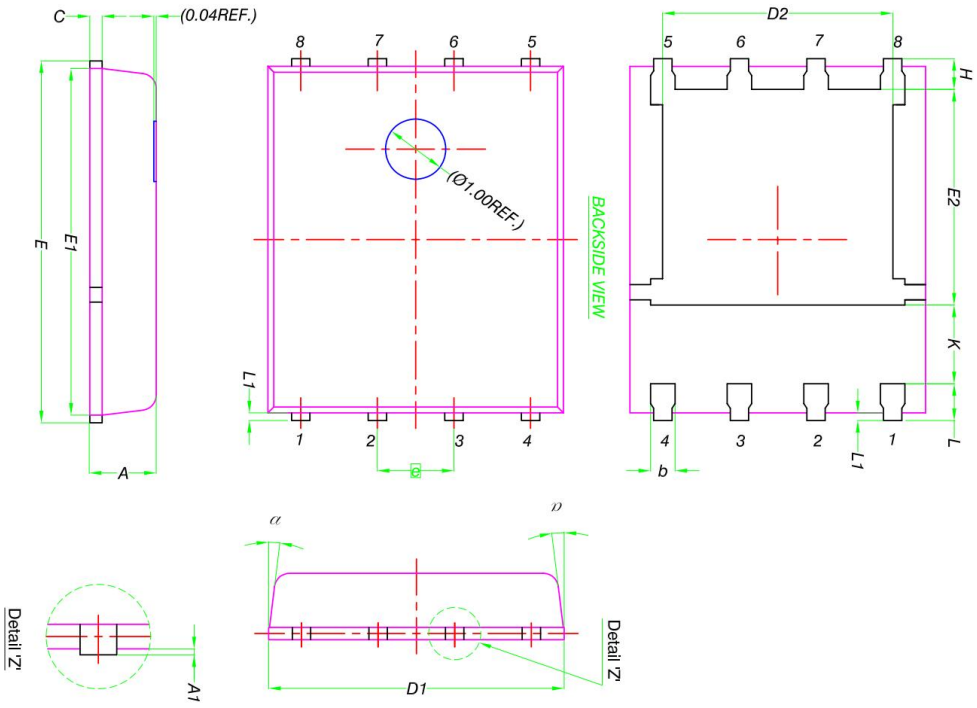
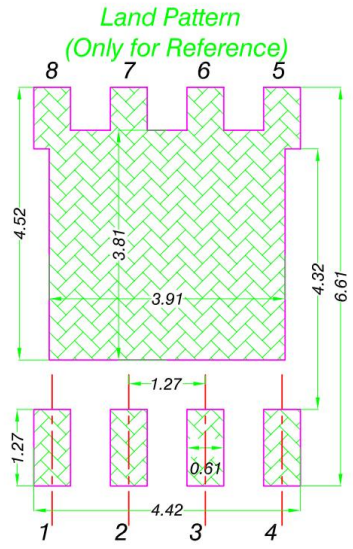


Figure 11 Normalized Maximum Transient Thermal Impedance

DFN5X6-8L(G) Package Information

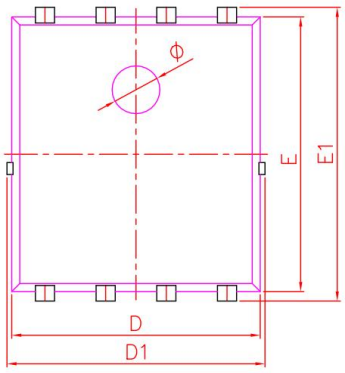


DIM.	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.90	1.00	1.10
A1	0	-	0.05
b	0.33	0.41	0.51
C	0.20	0.25	0.30
D1	4.80	4.90	5.00
D2	3.61	3.81	3.96
E	5.90	6.00	6.10
E1	5.70	5.75	5.80
E2	3.38	3.58	3.78
e	1.27 BSC		
H	0.41	0.51	0.61
K	1.10	-	-
L	0.51	0.61	0.71
L1	0.06	0.13	0.20
α	0°	-	12°

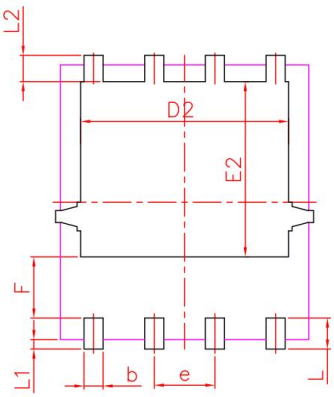


Note:
1. All Dimension Are In mm.
2. Package Body Sizes Exclude Mold Flash, Protrusion Or Gate Burrs.
   Mold Flash, Protrusion Or Gate Burrs Shall Not Exceed 0.10 mm Per Side.
3. Package Body Sizes Determined At The Outermost Extremes Of The Plastic
   Body Exclusive Of Mold Flash, Tie Bar , Tie Bar Burrs, Gate Burrs And Interlead Flash,
   But Including Any Mismatch Between The Top And Bottom Of The Plastic Body.
4. The Package Top May Be Smaller Than The Package Bottom.

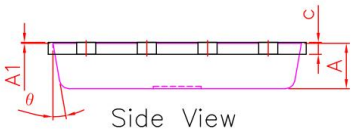
DFN5X6-8L(E) Package Information



Top View



Bottom View



Side View

PDFN5X6-8L			
DIM.	MIN.	NOM.	MAX.
A	0.90	0.95	1.00
A1	0.00	0.02	0.05
b	0.35	0.40	0.50
c	0.20	0.25	0.30
D	5.10	5.20	5.30
D1	5.10	5.40	5.50
D2	4.25	4.35	4.45
e	1.27 BSC		
E	5.70	5.75	5.80
E1	6.00	6.15	6.30
E2	3.57	3.67	3.77
F	1.18	1.28	1.38
L	0.55	0.65	0.75
L1	0.15	0.20	0.25
L2	0.45	0.55	0.65
ø	0.90	1.00	1.10
Θ	8°	10°	12°
All dimensions in millimeters			

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