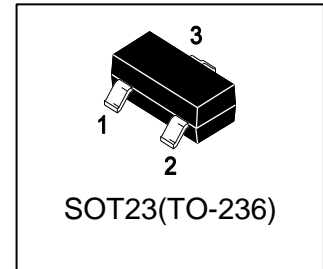


LP2128LT1G

20V P-Channel Enhancement-Mode MOSFET

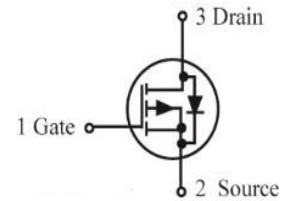
1. FEATURES

- $V_{DS} = -20V$
- Advanced trench process technology
- High Density Cell Design For Ultra Low On-Resistance
- Fully Characterized Avalanche Voltage and Current
- We declare that the material of product compliance with RoHS requirements and Halogen Free.



2. APPLICATIONS

- Simple Drive Requirement
- Small Package Outline
- Surface Mount Device



3. DEVICE MARKING AND ORDERING INFORMATION

Device	Marking	Shipping
LP2128LT1G	PA2	3000/Tape&Reel
LP2128LT3G	PA2	10000/Tape&Reel

4. MAXIMUM RATINGS($T_a = 25^\circ C$)

Parameter	Symbol	Limits	Unit
Drain-Source Voltage	V_{DSS}	-20	V
Gate-to-Source Voltage	V_{GS}	± 12	V
Drain Current(Note 1)			A
- Continuous $T_A = 25^\circ C$	I_D	-6	
- Pulsed	I_{DM}	-24	
Avalanche Current($L=0.1mH$)	I_{AS}	12	A
Avalanche Energy($L=0.1mH$)	E_{AS}	7.3	mJ

5. THERMAL CHARACTERISTICS

Parameter	Symbol	Limits	Unit
Power Dissipation (Note 2)	PD	1.1	W
Maximum Junction-to-Ambient (Note 2)	$R_{\theta JA}$	110	$^\circ C/W$
Junction and Storage temperature	T_J, T_{stg}	$-55 \sim +150$	$^\circ C$

1.Repetitive Rating: Pulse width limited by the maximum junction temperature.

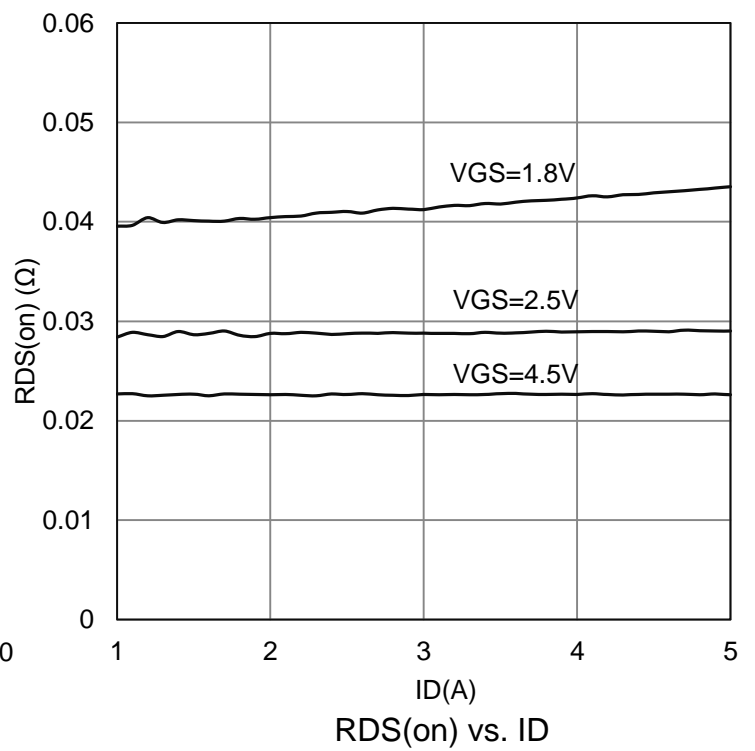
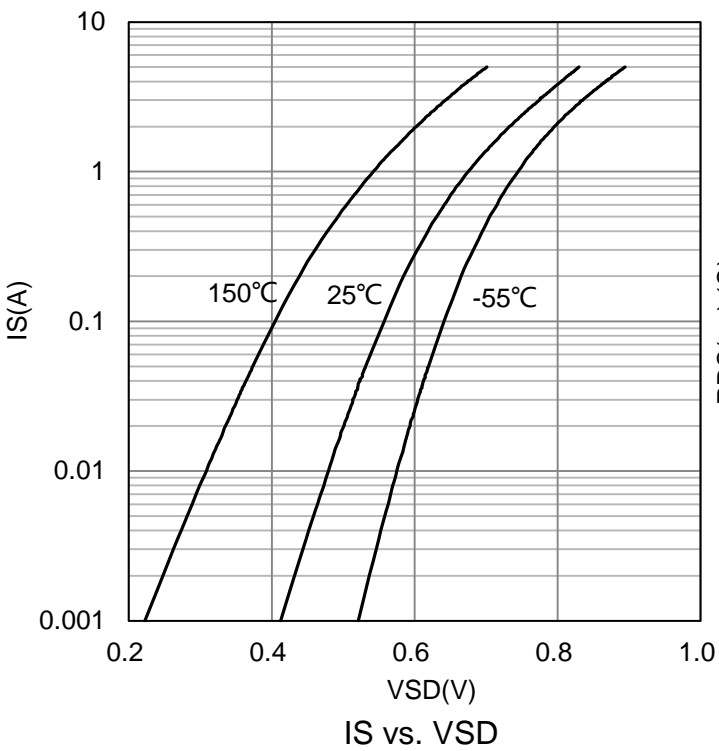
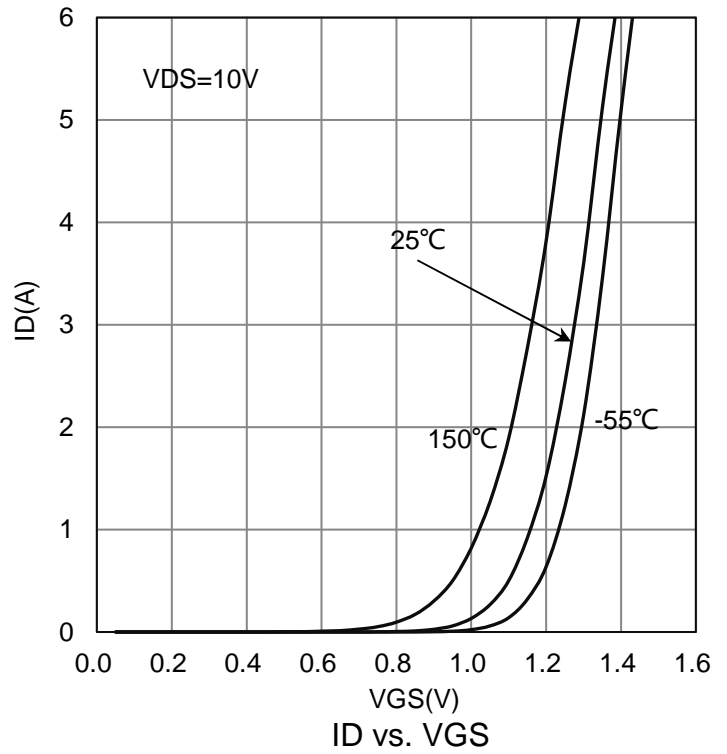
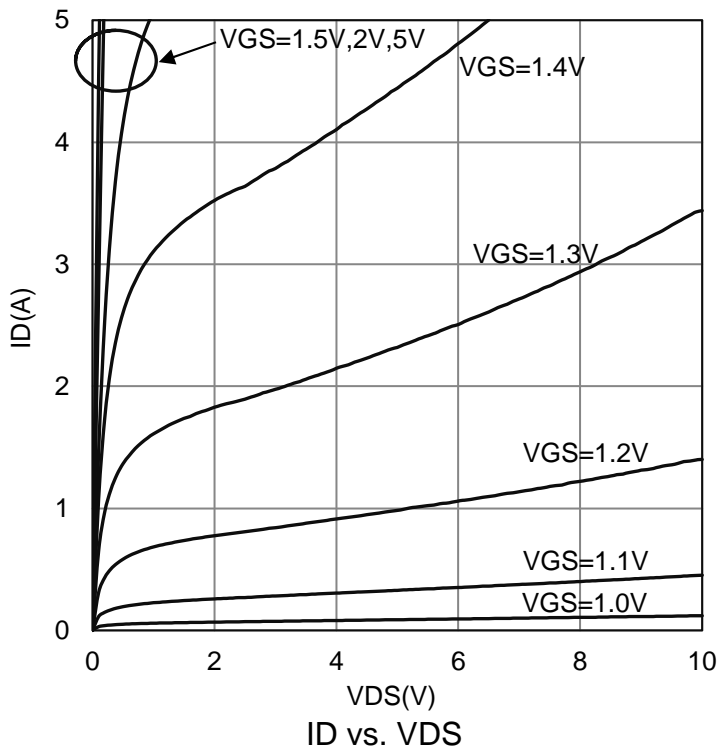
2.Surface mounted on "1.5 x 1.5" FR4 board using 1 sq in pad, 2 oz Cu.

6. ELECTRICAL CHARACTERISTICS (Ta= 25°C)

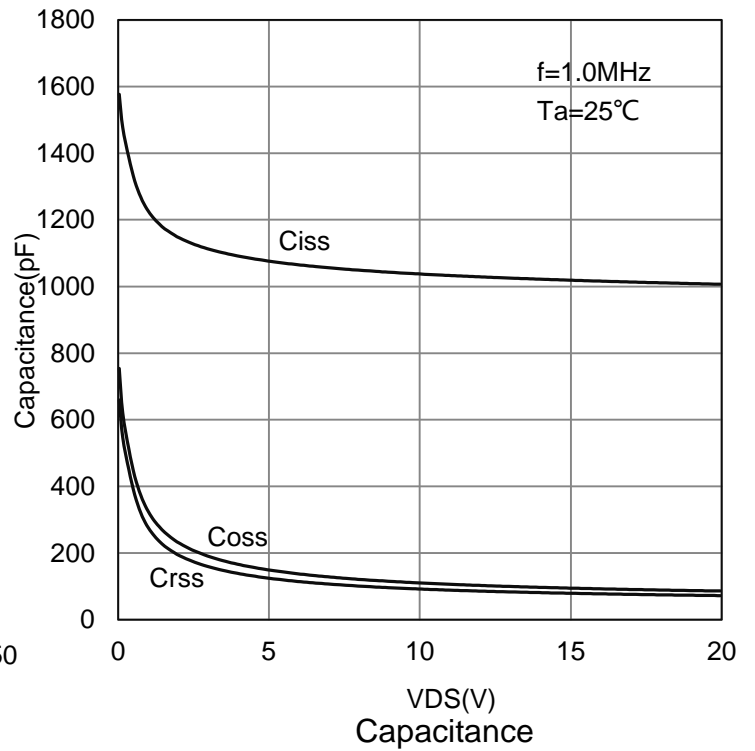
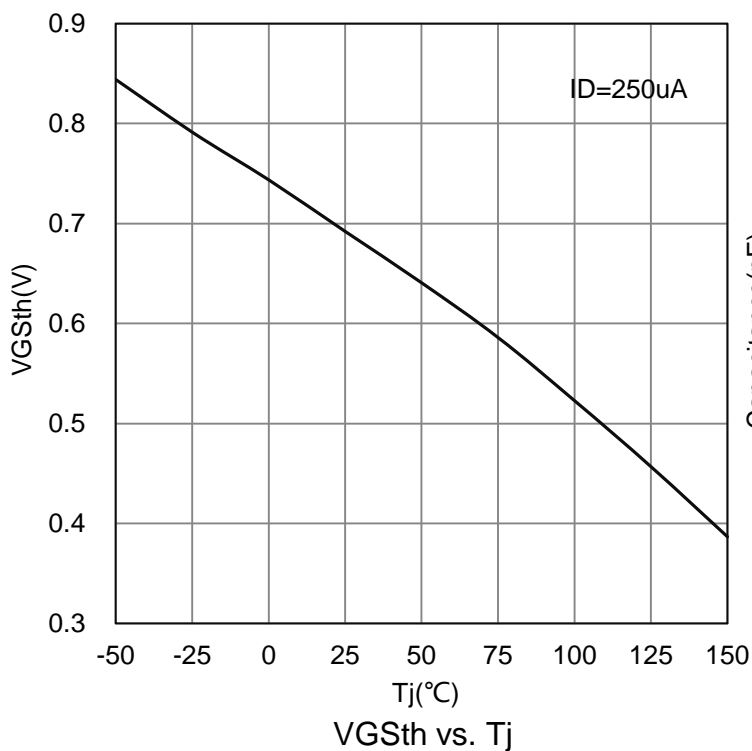
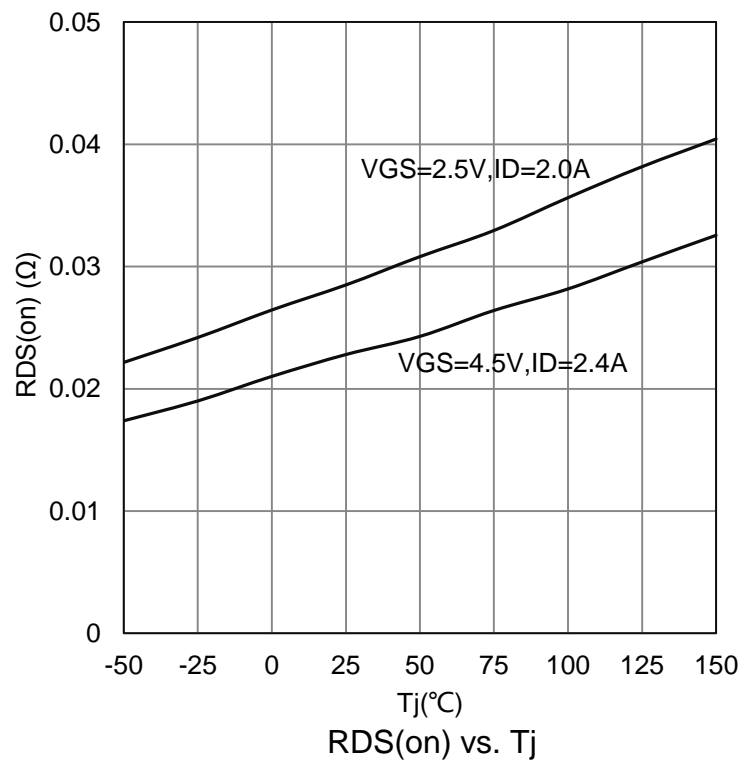
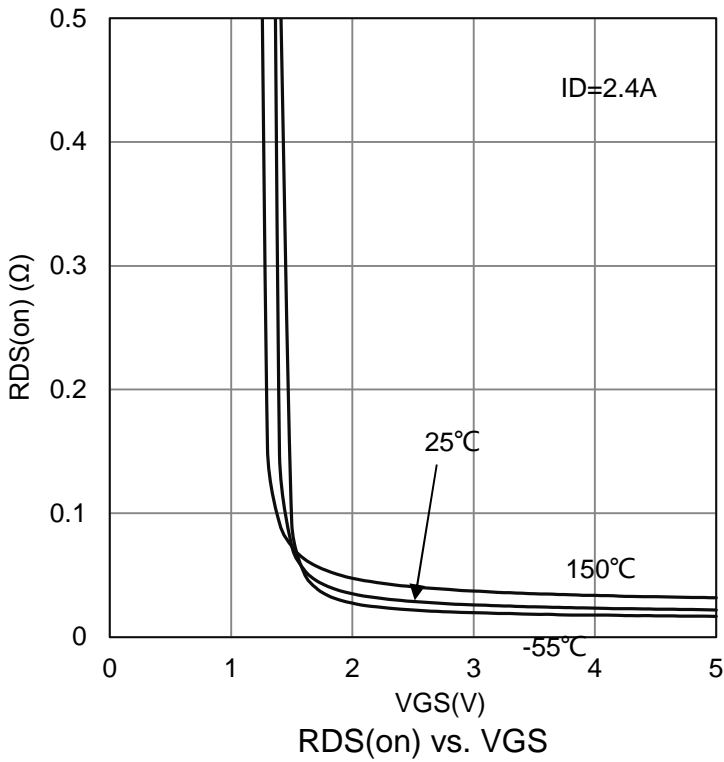
Characteristic	Symbol	Min.	Typ.	Max.	Unit	
Static						
Drain–Source Breakdown Voltage (VGS = 0, ID = -250μA)	VBRDSS	-20	-	-	V	
Zero Gate Voltage Drain Current (VGS = 0, VDS = -20 V)	IDSS	-	-	-1	μA	
Gate–Body Leakage Current (VGS = ±12 V, VDS=0V)	IGSS	-	-	±100	nA	
Gate Threshold Voltage (VDS = VGS, ID = -250μA)	VGS(th)	-0.45	-	-0.9	V	
Static Drain–Source On–State Resistance (VGS = -4.5 V, ID = -2.4 A) (VGS = -2.5 V, ID = -2 A) (VGS = -1.8 V, ID = -1 A)	RDS(on)	-	17 25 47	28 41 78	mΩ	
Dynamic(Note 3)						
Input Capacitance (VGS = 0 V, f = 1.0MHz, VDS= -4 V)	Ciss	-	1038	-	pF	
Output Capacitance (VGS = 0 V, f = 1.0MHz, VDS= -4 V)	Coss	-	110	-	pF	
Reverse Transfer Capacitance (VGS = 0 V, f = 1.0MHz, VDS= -4 V)	Crss	-	92	-	pF	
Total Gate Charge	(VDS=-10V, VGS=-4.5V, ID=-2.4A)	Qg	-	11	-	nC
Gate to Source Charge		Qgs	-	1.7	-	
Gate to Drain Charge		Qgd	-	2.5	-	
Turn-On Delay Time	(VDD=-4V, RL=4Ω, RG=6.2Ω, VGEN=-4.5V, ID=-1A)	td(on)	-	6.2	-	ns
Rise Time		tr	-	14.4	-	
Turn-Off Delay Time		td(off)	-	46	-	
Fall Time		tf	-	24	-	
Diode Forward Voltage (IS = -1.6A, VGS = 0V)	VSD	-	-	-1.2	V	

3.Pulse Test: Pulse Width ≤300 μs, Duty Cycle ≤2.0%.

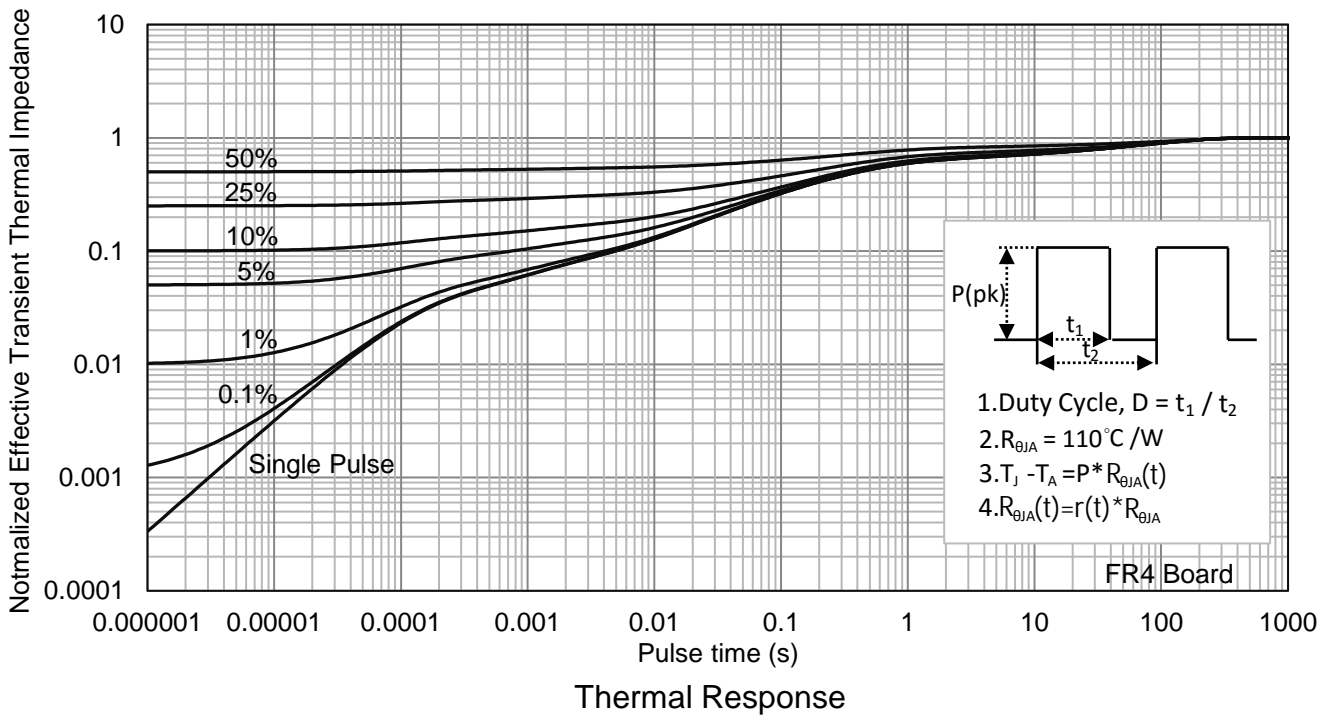
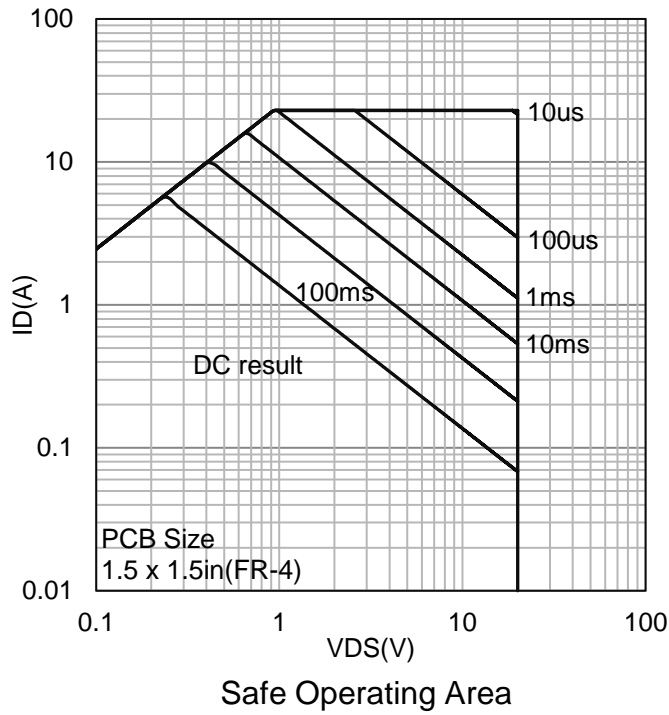
7. ELECTRICAL CHARACTERISTICS CURVES



7.ELECTRICAL CHARACTERISTICS CURVES(Con.)



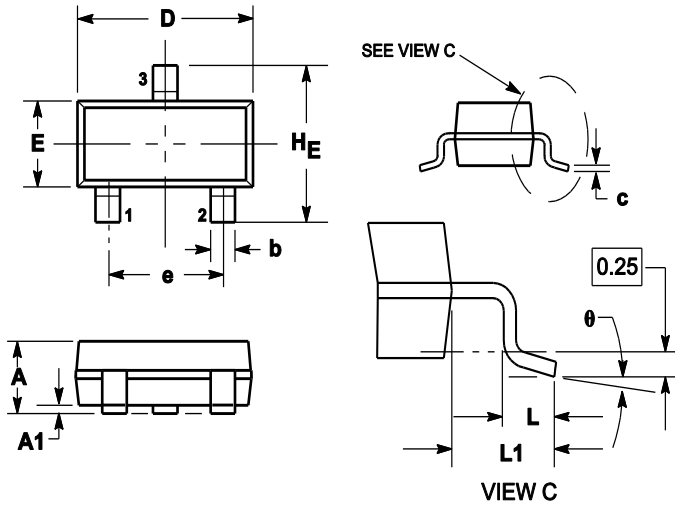
7.ELECTRICAL CHARACTERISTICS CURVES(Con.)



8. OUTLINE AND DIMENSIONS

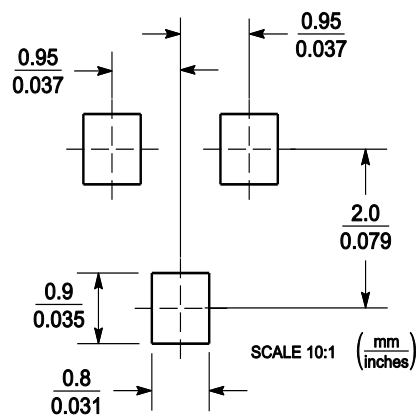
Notes:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.



DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.89	1	1.11	0.035	0.04	0.044
A1	0.01	0.06	0.1	0.001	0.002	0.004
b	0.37	0.44	0.5	0.015	0.018	0.02
c	0.09	0.13	0.18	0.003	0.005	0.007
D	2.80	2.9	3.04	0.11	0.114	0.12
E	1.20	1.3	1.4	0.047	0.051	0.055
e	1.78	1.9	2.04	0.07	0.075	0.081
L	0.10	0.2	0.3	0.004	0.008	0.012
L1	0.35	0.54	0.69	0.014	0.021	0.029
HE	2.10	2.4	2.64	0.083	0.094	0.104
theta	0°	---	10°	0°	---	10°

9. SOLDERING FOOTPRINT



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