# CoreGaN 650V GaN HEMT

Description	General Features
The CE65D150DNBI Series 650V, 150mΩ gallium nitride (GaN) FETs are normally-on devices. Corenergy GaN FETs offer better efficiency through lower gate charge, faster switching speeds, and zero reverse recovery charge, delivering significant advantages over traditional silicon (Si) devices. Corenergy is a leading-edge wide band gap supplier with world-class innovation .	Easy to drive—compatible with standard gate drivers Low conduction and switching losses RoHS compliant and Halogen-free
Application	**Benefits**
Fast charger Renewable energy Telecom and data-com Servo motors Industrial Automotive	Increased efficiency through fast switching Increased power density Reduced system size and weight
Valid Date: 02/06/2021	

Ordering Information

Part Number	Package	Package Configuration
CE65D150DNBI	PDFN	Source

Top   **Bottom**   **Circuit Symbol**
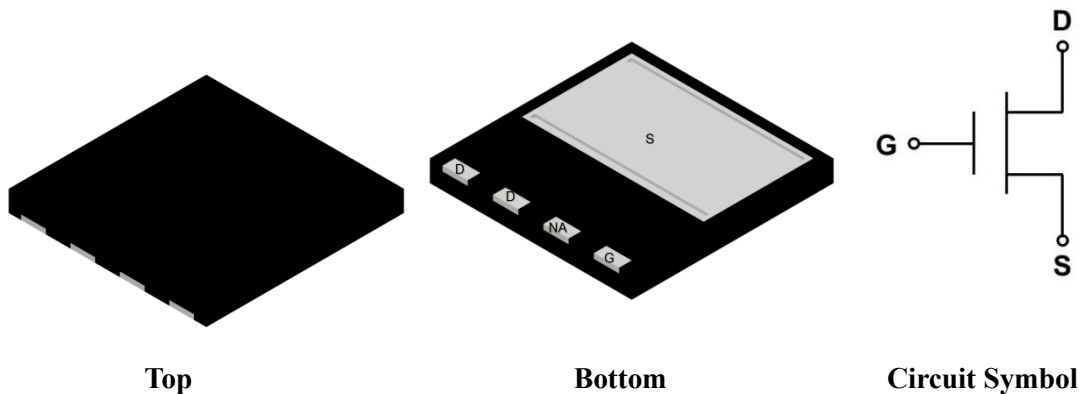
Absolute Maximum Ratings (T$_C$=25°C unless otherwise stated)

Symbol	Parameter	Limit value	Unit
V$_{DSS}$	Drain to source voltage (T$_J$ = -55°C to 150°C)	650	V
V$_{(TR)DSS}$	Drain to source voltage-transient [a]	900	
V$_{GSS}$	Gate to source voltage	-35~+10	

I_D	Continuous drain current @T_C=25°C [b]	15	A
	Continuous drain current @T_C=150°C [b]	10	
I_{DM}	Pulse drain current (pulse width: 100μs)	40	A
P_D	Maximum power dissipation @ T_C=25°C	65	W
T_C	Operating temperature	Case	-55~150	°C
T_J		Junction	-55~150	°C
T_S	Storage temperature	-55~150	°C

Notes:

a. In off-state, spike duty cycle D<0.01, spike duration <1μs

b. For increased stability at high current operation

Thermal Resistance

Symbol	Parameter	Limit value	Unit
$R_{θJC}$	Junction-to-case	1.3	°C /W

Electrical Parameters (T_J=25°C unless otherwise stated)

| Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
Forward Device Characteristics						
$V_{(BL)DSS}$	Drain-source voltage	650	-	-	V	V_{GS}= -25V
$V_{GS(th)}$	Gate threshold voltage		-18		V	V_{DS}=V_{GS}, I_{DS}=1uA
$\triangle V_{GS(th)}/T_J$	Gate threshold voltage temperature coefficient		-22		mV/°C	
$R_{DS(on)}$	Drain-source on-resistance	-	150	200	mΩ	V_{GS}=0V, I_D=10A, T_J=25°C
		-	280	-		V_{GS}=0V, I_D=10A, T_J=150°C
I_{DSS}	Drain-to-source leakage current	-	-	0.2	uA	V_{DS}=650V, V_{GS}= -25V, T_J=25°C
		-	-	1		V_{DS}=650V, V_{GS}= -25V, T_J=150°C
I_{GSS}	Gate-to-source forward leakage current	-	-	10	nA	V_{GS}=-25V
C_{ISS}	Input capacitance	-	69	-	pF	V_{GS}=-25V, V_{DS}=400V, f=1MHz
C_{OSS}	Output capacitance	-	24	-		
C_{RSS}	Reverse capacitance	-	7	-		
Q_G	Total gate charge	-	22	-	nC	V_{DS}=400V, V_{GS}=-25V to 0V, I_D=1A
Q_{GS}	Gate-source charge	-	2.4	-		
Q_{GD}	Gate-drain charge	-	15	-		
Q_{OSS}	Output charge		22		nC	V_{GS}=-25V, V_{DS}=0V to 400V, f=1MHz
$t_{D(on)}$	Turn-on delay	-	5	-	ns	V_{DS}=400V, V_{GS}=-25V to 0V, I_D=10A
t_R	Rise time	-	16	-		
$t_{D(off)}$	Turn-off delay	-	6	-		
t_F	Fall time	-	14	-		

Typical Characteristics (T_J=25°C unless otherwise stated)
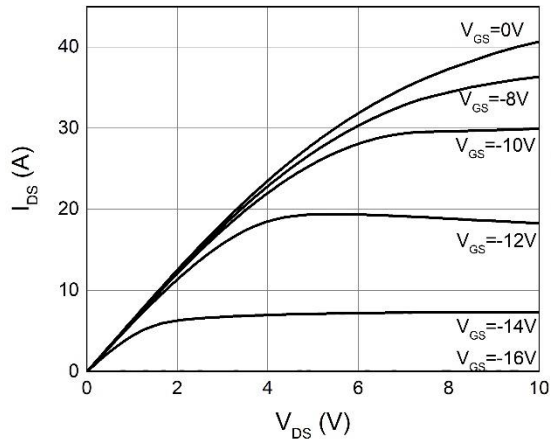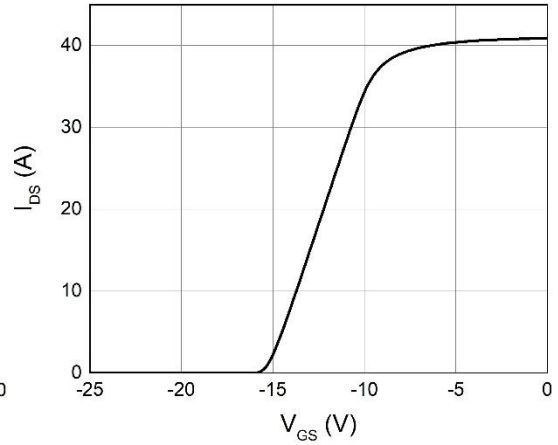
Figure 1. Typical Output Characteristics T_J=25°C

Figure 2. Typical Transfer Characteristics T_J=25°C
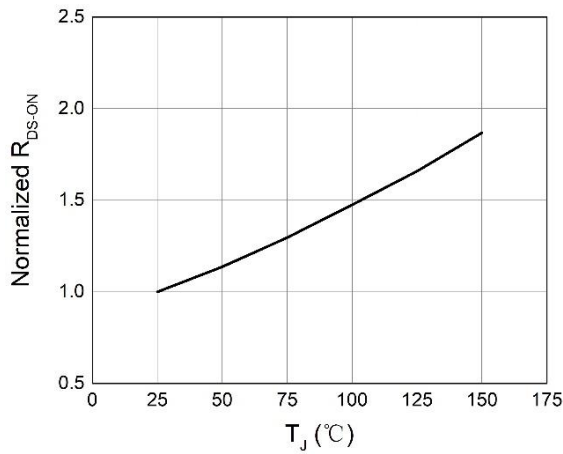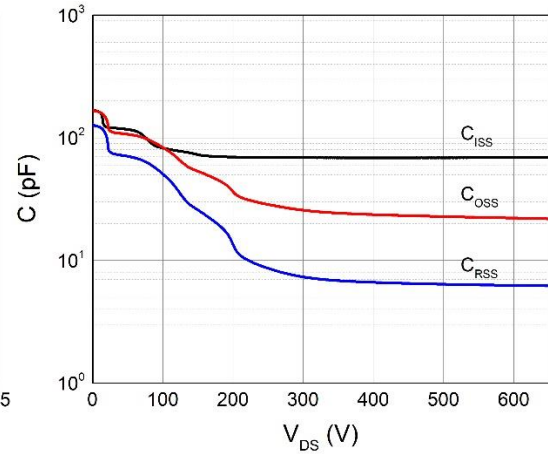
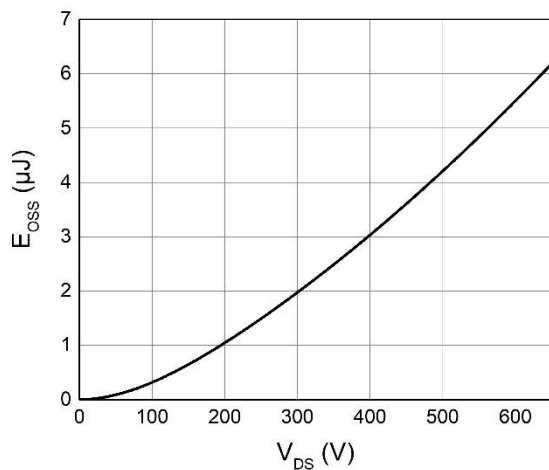Figure 3. Normalized On-resistance

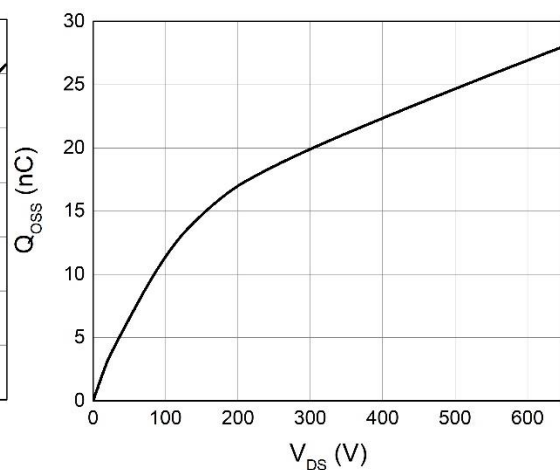Figure 4. Typical Capacitance

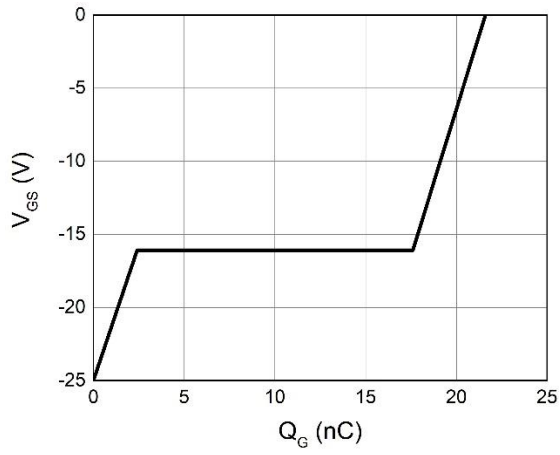Figure 5. Typical C_OSS Stored Energy

Figure 6. Typical Q_OSS

Figure 7. Typical Gate Charge

PACKAGE DIMENSIONS

DFN8*8-4L-A

Document No.	
Version	A

DFN8x8_4L PACKAGE OUTLINE

Top view

S

Pin1 dot:R0.15

G

Bottom view

S

N/A

D D G

Side view

ITEM	Low limit (mm)	Center (mm)	Upper limit (mm)
A	0.80	0.90	1.00
A1	0		0.05
A2	0.15	0.25	0.35
b	0.9	1	1.1
D	7.9	8	8.1
D1	6.9	7	7.1
D2	0.4	0.5	0.6
D3	7.1	7.2	7.3
D4	0.3	0.4	0.5
E	7.9	8	8.1
E1	0.3	0.4	0.5
E2	4.25	4.35	4.45
E3	2.65	2.75	2.85
e	1.9	2	2.1
L	0.4	0.5	0.6

NOTE
CONTROLLING DIMENSION IS MILLIMETER.
CONVERTED INCH DIMENSIONS ARE NOT NECESSARILY EXACT.