

N-Channel 80 V (D-S) MOSFET

PRODUCT SUMMARY			
V _{DS} (V)	R _{DS(on)} (Ω) MAX.	I _D (A)	Q _g (TYP.)
80	0.0050 at V _{GS} = 10 V	215	94
	0.0095 at V _{GS} = 7.5 V	205	

FEATURES

- TrenchFET® power MOSFET
- Maximum 175 °C junction temperature
- Very low Q_{gd} reduces power loss from passing through V_{plateau}
- 100 % R_G and UIS tested

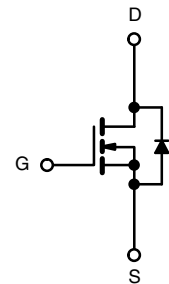


RoHS
COMPLIANT
HALOGEN
FREE



APPLICATIONS

- Power supply
- Secondary synchronous rectification
- DC/DC converter
- Power tools
- Motor drive switch
- DC/AC inverter
- Battery management



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS (T _C = 25 °C, unless otherwise noted)			
PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	V _{DS}	80	V
Gate-Source Voltage	V _{GS}	± 20	
Continuous Drain Current (T _J = 150 °C)	I _D	T _C = 25 °C	215
		T _C = 70 °C	120 ^d
Pulsed Drain Current (t = 100 μs)	I _{DM}	600	A
Avalanche Current	I _{AS}	70	
Single Avalanche Energy ^a	E _{AS}	245	mJ
Maximum Power Dissipation ^a	P _D	T _C = 25 °C	375 ^b
		T _C = 125 °C	125 ^b
Operating Junction and Storage Temperature Range	T _J , T _{stg}	-55 to +175	°C

THERMAL RESISTANCE RATINGS			
PARAMETER	SYMBOL	LIMIT	UNIT
Junction-to-Ambient (PCB Mount) ^c	R _{thJA}	40	°C/W
Junction-to-Case (Drain)	R _{thJC}	0.4	

Notes

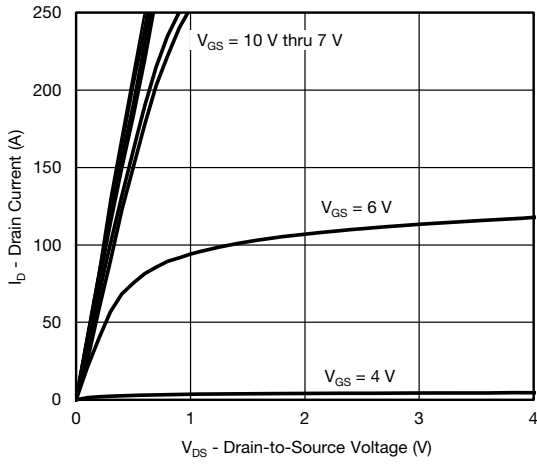
- Duty cycle ≤ 1 %.
- See SOA curve for voltage derating.
- When mounted on 1" square PCB (FR4 material).
- Package limited.

SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0 V, I _D = 250 μA	80	-	-	V
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	2	-	4	
Gate-Body Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 20 V	-	-	± 250	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 80 V, V _{GS} = 0 V	-	-	1	μA
		V _{DS} = 80 V, V _{GS} = 0 V, T _J = 125 °C	-	-	150	
		V _{DS} = 80 V, V _{GS} = 0 V, T _J = 175 °C	-	-	5	mA
On-State Drain Current ^a	I _{D(on)}	V _{DS} ≥ 10 V, V _{GS} = 10 V	120	-	-	A
Drain-Source On-State Resistance ^a	R _{DS(on)}	V _{GS} = 10 V, I _D = 30 A	-	0.0050	-	Ω
		V _{GS} = 7.5 V, I _D = 20 A	-	0.0095	-	
Forward Transconductance ^a	g _{fs}	V _{DS} = 15 V, I _D = 30 A	-	82	-	S
Dynamic ^b						
Input Capacitance	C _{iss}	V _{GS} = 0 V, V _{DS} = 40 V, f = 1 MHz	-	7910	-	pF
Output Capacitance	C _{oss}		-	3250	-	
Reverse Transfer Capacitance	C _{rss}		-	348	-	
Total Gate Charge ^c	Q _g	V _{DS} = 40 V, V _{GS} = 10 V, I _D = 20 A	-	94	141	nC
Gate-Source Charge ^c	Q _{gs}		-	31	-	
Gate-Drain Charge ^c	Q _{gd}		-	10	-	
Gate Resistance	R _g	f = 1 MHz	0.28	1.4	2.8	Ω
Turn-On Delay Time ^c	t _{d(on)}	V _{DD} = 40 V, R _L = 4 Ω I _D ≅ 10 A, V _{GEN} = 10 V, R _g = 1 Ω	-	24	40	ns
Rise Time ^c	t _r		-	24	40	
Turn-Off Delay Time ^c	t _{d(off)}		-	34	60	
Fall Time ^c	t _f		-	14	28	
Drain-Source Body Diode Ratings and Characteristics ^b (T_C = 25 °C)						
Pulsed Current (t = 100 μs)	I _{SM}		-	-	250	A
Forward Voltage ^a	V _{SD}	I _F = 10 A, V _{GS} = 0 V	-	0.8	1.5	V
Reverse Recovery Time	t _{rr}	I _F = 34 A, di/dt = 100 A/μs	-	126	190	ns
Peak Reverse Recovery Charge	I _{RM(REC)}		-	5	10	A
Reverse Recovery Charge	Q _{rr}		-	0.315	0.475	μC

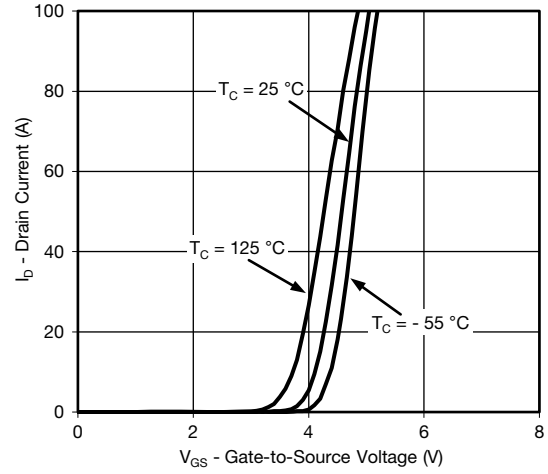
Notes

- a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2 %.
- b. Guaranteed by design, not subject to production testing.
- c. Independent of operating temperature.

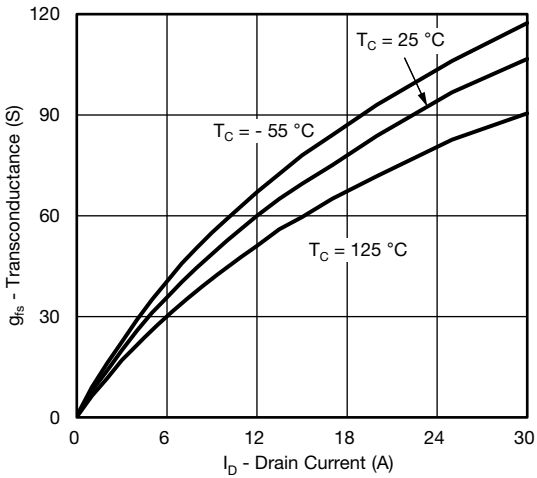
TYPICAL CHARACTERISTICS ($T_A = 25\text{ }^\circ\text{C}$, unless otherwise noted)



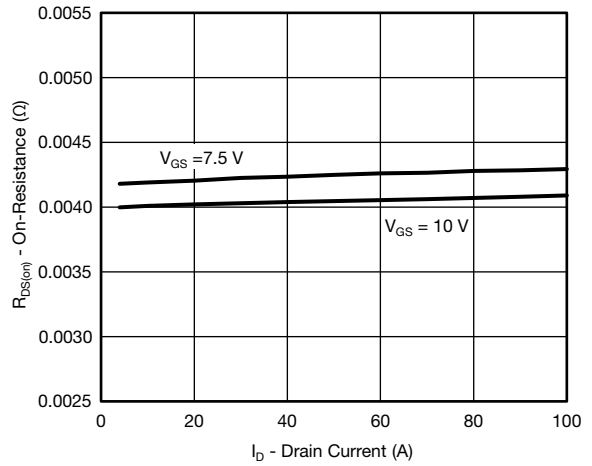
Output Characteristics



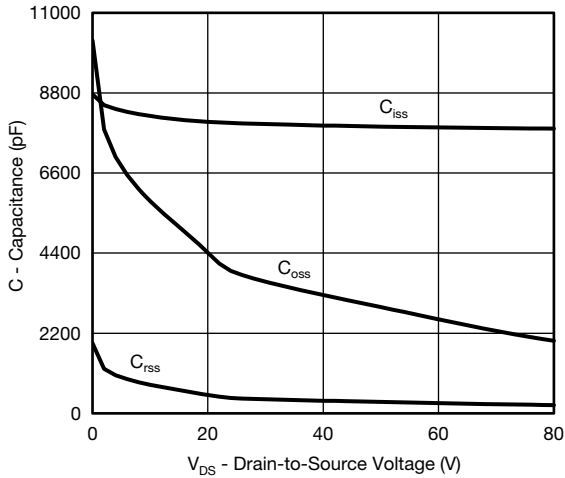
Transfer Characteristics



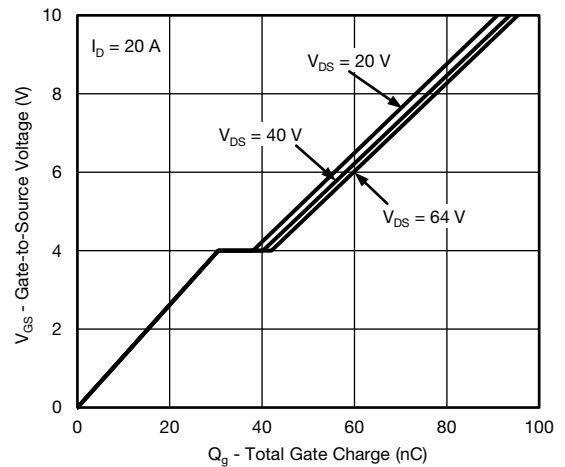
Transconductance



On-Resistance vs. Drain Current

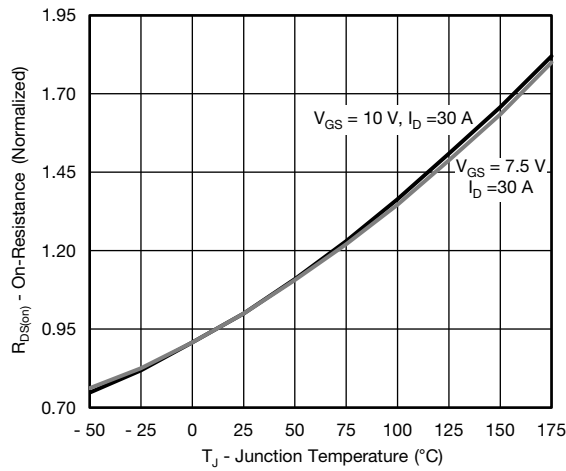


Capacitance

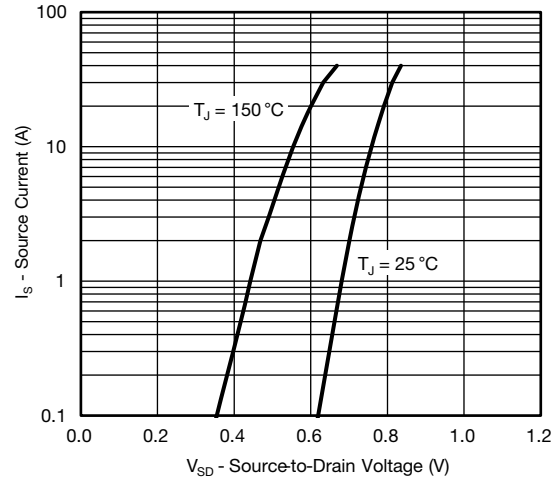


Gate Charge

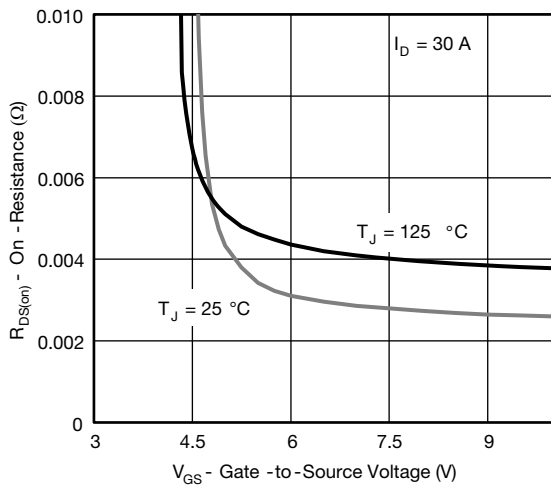
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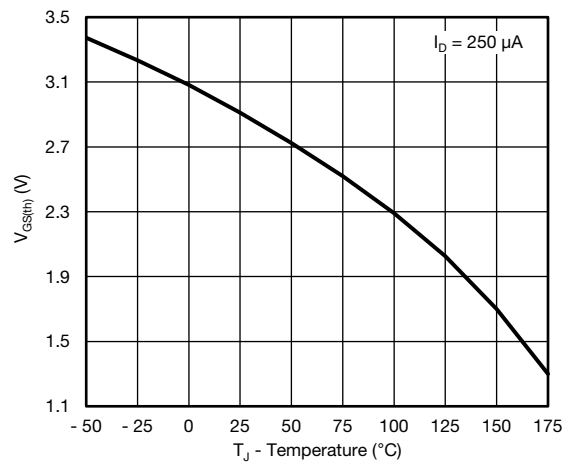
On-Resistance vs. Junction Temperature



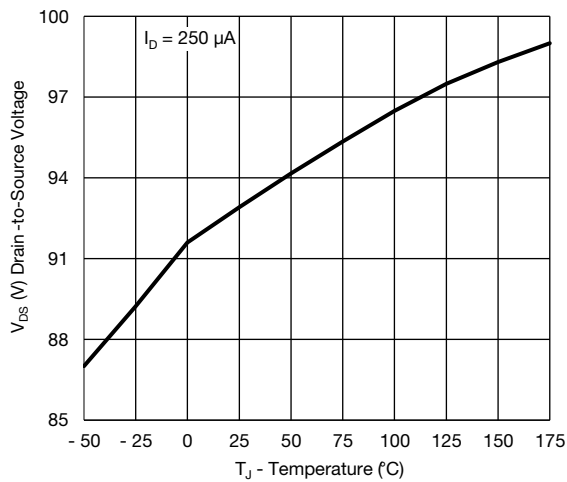
Source Drain Diode Forward Voltage



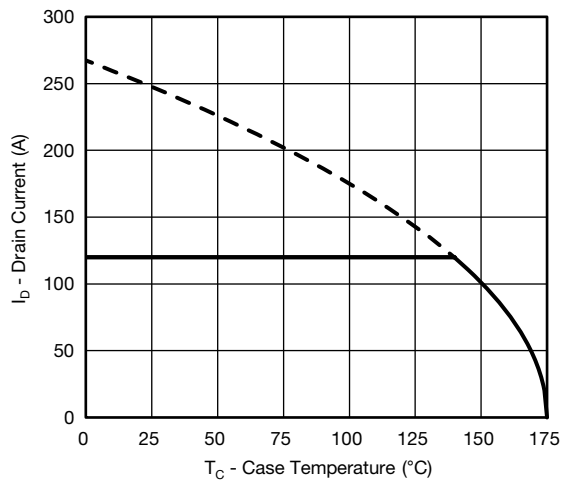
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage

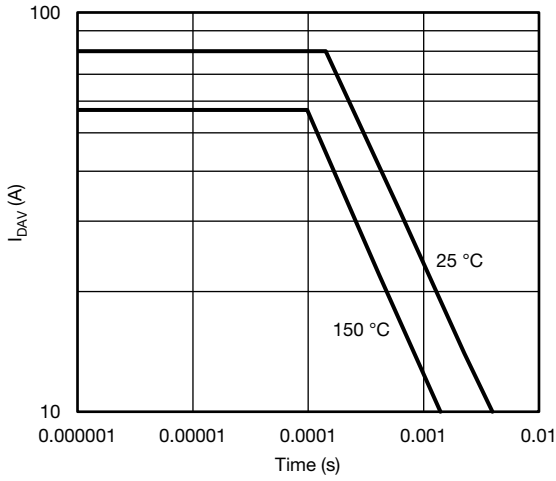


Drain Source Breakdown vs. Junction Temperature

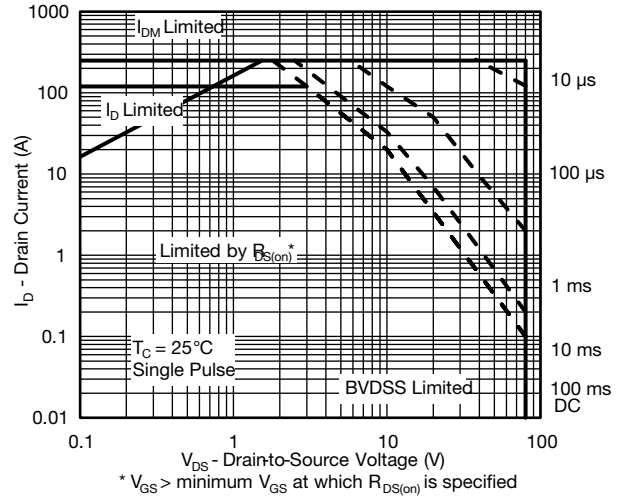


Current De-rating

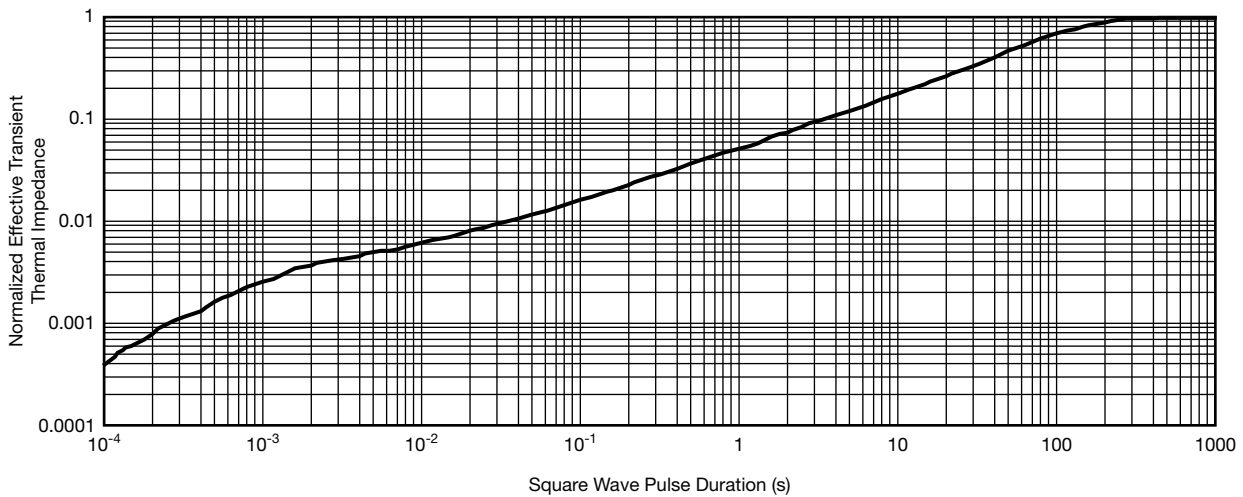
THERMAL RATINGS ($T_A = 25\text{ }^\circ\text{C}$, unless otherwise noted)



Single Pulse Avalanche Current Capacity vs. Time

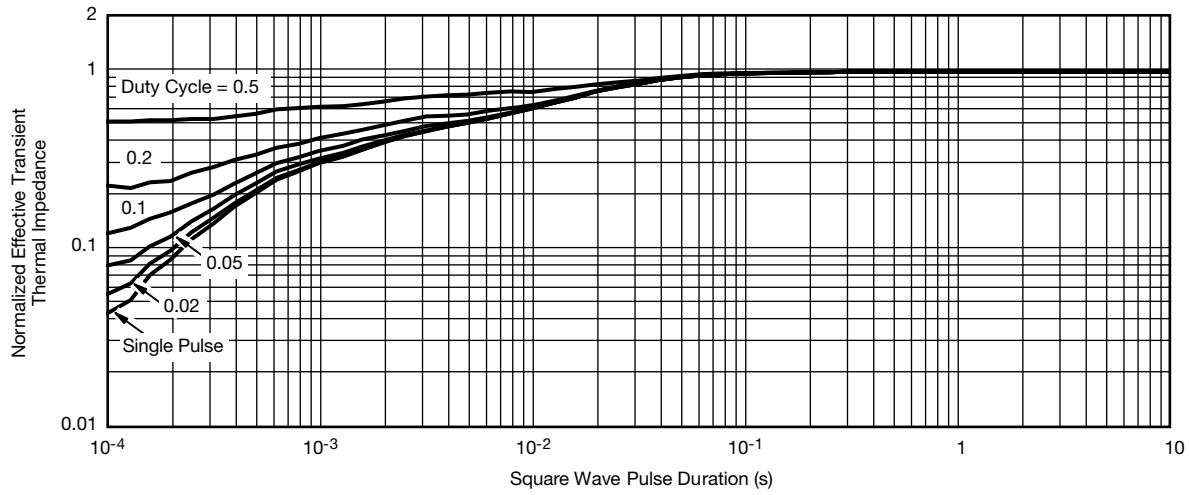


Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Ambient

THERMAL RATINGS ($T_A = 25\text{ }^\circ\text{C}$, unless otherwise noted)

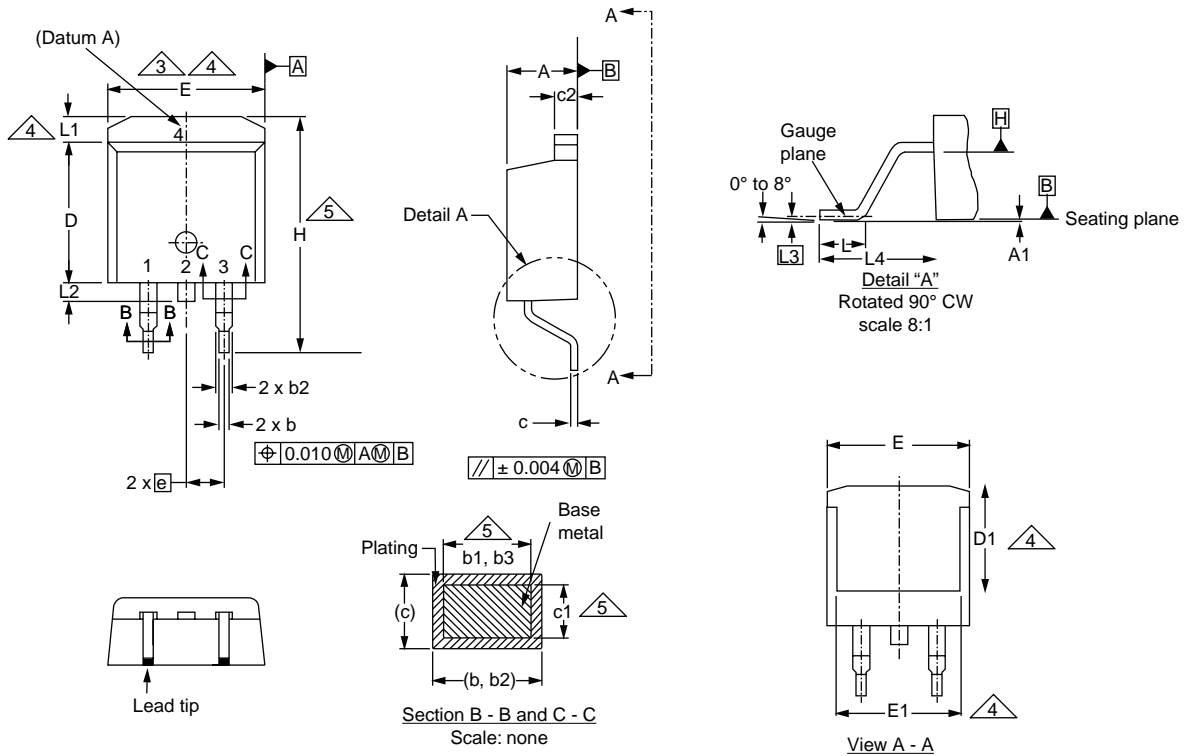


Normalized Thermal Transient Impedance, Junction-to-Case

Note

- The characteristics shown in the two graphs
 - Normalized Transient Thermal Impedance Junction to Ambient (25 °C)
 - Normalized Transient Thermal Impedance Junction to Case (25 °C)
- are given for general guidelines only to enable the user to get a “ball park” indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board - FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions.

TO-263AB



DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	4.06	4.83	0.160	0.190
A1	0.00	0.25	0.000	0.010
b	0.51	0.99	0.020	0.039
b1	0.51	0.89	0.020	0.035
b2	1.14	1.78	0.045	0.070
b3	1.14	1.73	0.045	0.068
c	0.38	0.74	0.015	0.029
c1	0.38	0.58	0.015	0.023
c2	1.14	1.65	0.045	0.065
D	8.38	9.65	0.330	0.380

DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
D1	6.86	-	0.270	-
E	9.65	10.67	0.380	0.420
E1	6.22	-	0.245	-
e	2.54 BSC		0.100 BSC	
H	14.61	15.88	0.575	0.625
L	1.78	2.79	0.070	0.110
L1	-	1.65	-	0.066
L2	-	1.78	-	0.070
L3	0.25 BSC		0.010 BSC	
L4	4.78	5.28	0.188	0.208

ECN: S-82110-Rev. A, 15-Sep-08
DWG: 5970

Notes

1. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. Dimensions are shown in millimeters (inches).
3. Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005") per side. These dimensions are measured at the outmost extremes of the plastic body at datum A.
4. Thermal PAD contour optional within dimension E, L1, D1 and E1.
5. Dimension b1 and c1 apply to base metal only.
6. Datum A and B to be determined at datum plane H.
7. Outline conforms to JEDEC outline to TO-263AB.

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