

## Dual N-Channel Advanced Power MOSFET

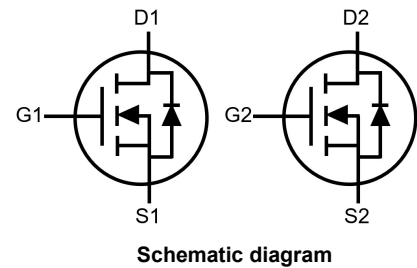
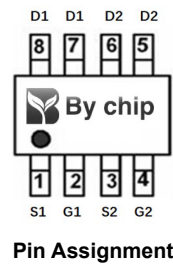
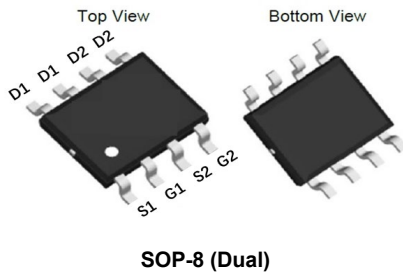
### Features

- $V_{DS} = 60V$ ,  $I_D = 5A$   
 $R_{DS(ON)} < 30\text{ m}\Omega @ V_{GS} = 10V$   
 $R_{DS(ON)} < 36\text{ m}\Omega @ V_{GS} = 4.5V$

### General Features

- Advanced Trench Technology
- Provide Excellent  $R_{DS(ON)}$  and Low Gate Charge
- Lead Free and Green Available

100% UIS TESTED!  
 100%  $\Delta V_{ds}$  TESTED!



### Absolute Maximum Ratings ( $T_A = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Max.	Units
$V_{DSS}$	Drain-Source Voltage	60	V
$V_{GSS}$	Gate-Source Voltage	$\pm 20$	V
$I_D$	Continuous Drain Current	$T_A = 25^\circ\text{C}$	5
		$T_A = 100^\circ\text{C}$	3.3
$I_{DM}$	Pulsed Drain Current <sup>note1</sup>	20	A
EAS	Single Pulsed Avalanche Energy <sup>note2</sup>	20	mJ
$P_D$	Power Dissipation	$T_A = 25^\circ\text{C}$	1.74
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	72	$^\circ\text{C}/\text{W}$
$T_J, T_{STG}$	Operating and Storage Temperature Range	-55 to +150	$^\circ\text{C}$

## Electrical Characteristics (T<sub>J</sub>=25°C unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
<b>Off Characteristics</b>						
V <sub>(BR)DSS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> =0V, I <sub>D</sub> =250μA	60	-	-	V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> =60V, V <sub>GS</sub> = 0V,	-	-	1.0	μA
I <sub>GSS</sub>	Gate to Body Leakage Current	V <sub>DS</sub> =0V, V <sub>GS</sub> = ±20V	-	-	±100	nA
<b>On Characteristics</b>						
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250μA	1.0		2.5	V
R <sub>DS(on)</sub>	Static Drain-Source on-Resistance <small>note3</small>	V <sub>GS</sub> =10V, I <sub>D</sub> =5A	-		30	mΩ
		V <sub>GS</sub> =4.5V, I <sub>D</sub> =3A	-		36	
<b>Dynamic Characteristics</b>						
C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> =25V, V <sub>GS</sub> =0V, f=1.0MHz	-	853	-	pF
C <sub>oss</sub>	Output Capacitance		-	60	-	pF
C <sub>rss</sub>	Reverse Transfer Capacitance		-	29	-	pF
Q <sub>g</sub>	Total Gate Charge	V <sub>DD</sub> =30V, I <sub>D</sub> =2.5A, V <sub>GS</sub> =10V	-	20	-	nC
Q <sub>gs</sub>	Gate-Source Charge		-	3	-	nC
Q <sub>gd</sub>	Gate-Drain("Miller") Charge		-	4.5	-	nC
<b>Switching Characteristics</b>						
t <sub>d(on)</sub>	Turn-on Delay Time	V <sub>DD</sub> =30V, I <sub>D</sub> =5A, R <sub>GEN</sub> =1.8Ω, V <sub>GS</sub> =10V	-	6	-	ns
t <sub>r</sub>	Turn-on Rise Time		-	6	-	ns
t <sub>d(off)</sub>	Turn-off Delay Time		-	19	-	ns
t <sub>f</sub>	Turn-off Fall Time		-	2.5	-	ns
<b>Drain-Source Diode Characteristics and Maximum Ratings</b>						
I <sub>S</sub>	Maximum Continuous Drain to Source Diode Forward Current		-	-	5	A
I <sub>SM</sub>	Maximum Pulsed Drain to Source Diode Forward Current		-	-	20	A
V <sub>SD</sub>	Drain to Source Diode Forward Voltage	V <sub>GS</sub> =0V, I <sub>S</sub> =5A	-	-	1.2	V
t <sub>rr</sub>	Body Diode Reverse Recovery Time	I <sub>F</sub> =5A, dI/dt=100A/μs	-	13	-	ns
Q <sub>rr</sub>	Body Diode Reverse Recovery Charge		-	9	-	nC

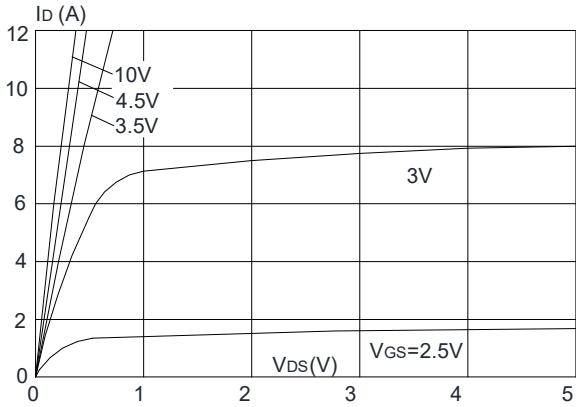
Notes:1. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature

2. EAS condition :Starting T<sub>J</sub>=25°C, V<sub>DD</sub>=30V, V<sub>GS</sub>=10V, L=0.5mH, R<sub>g</sub>=25Ω, I<sub>AS</sub>=9A

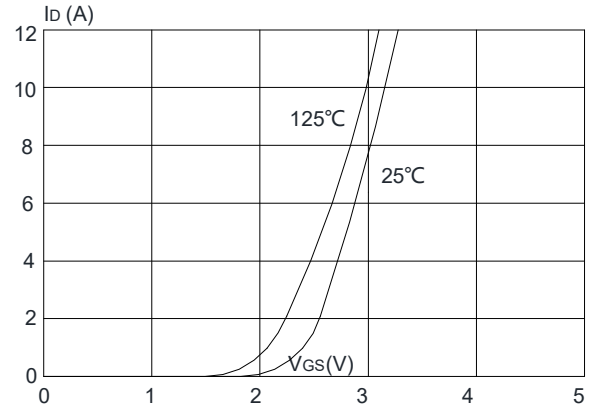
3. Pulse Test: Pulse Width≤300μs, Duty Cycle≤0.5%

## Typical Performance Characteristics

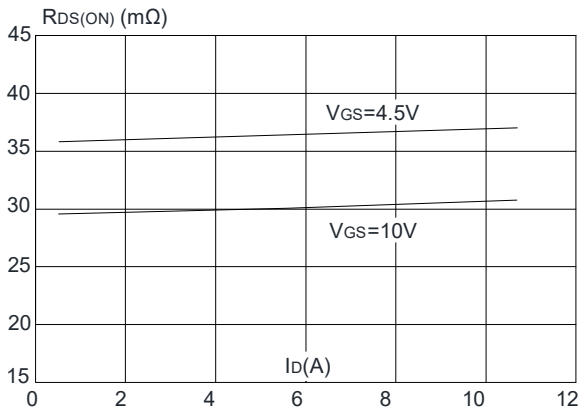
**Figure 1: Output Characteristics**



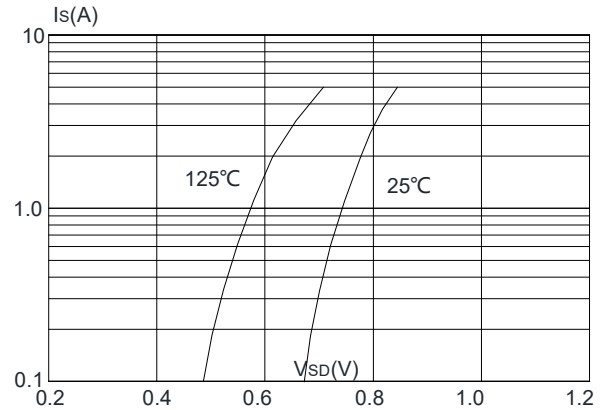
**Figure 2: Typical Transfer Characteristics**



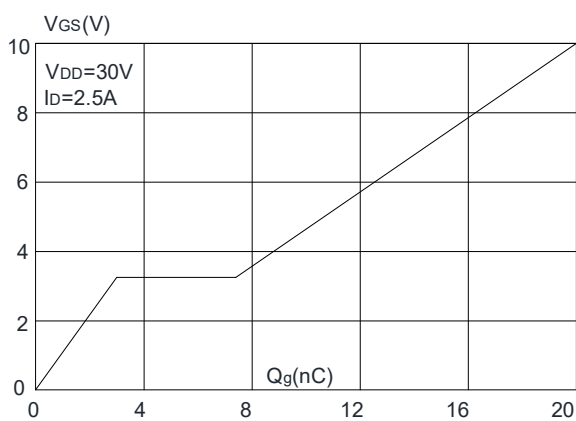
**Figure 3: On-resistance vs. Drain Current**



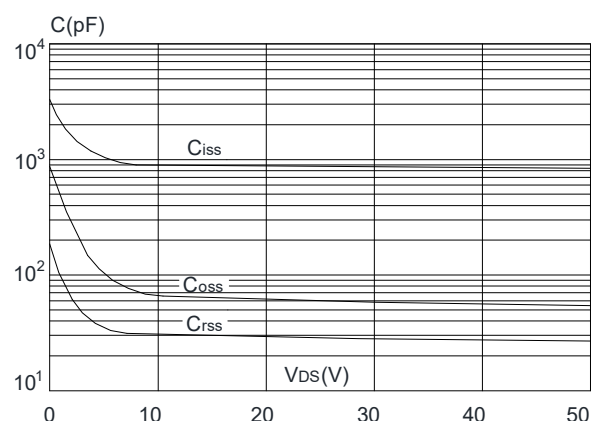
**Figure 4: Body Diode Characteristics**



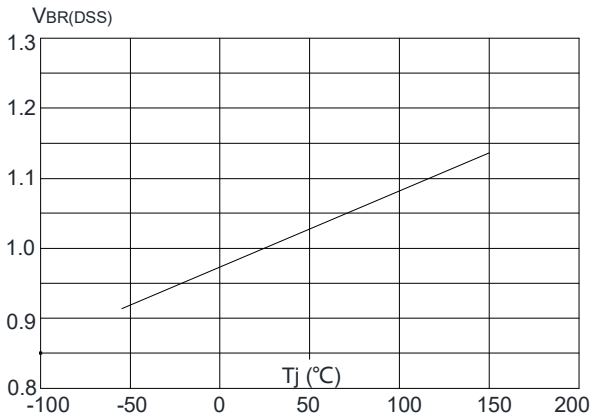
**Figure 5: Gate Charge Characteristics**



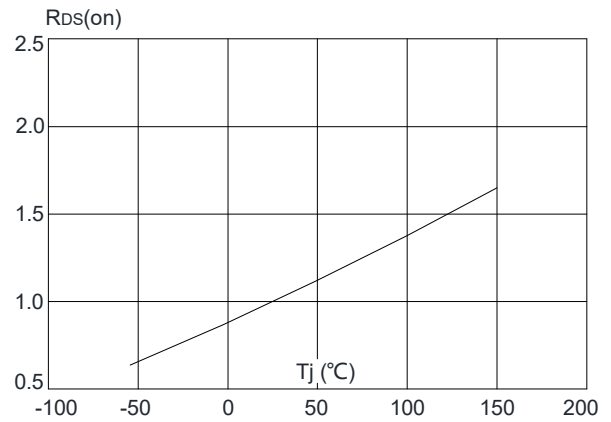
**Figure 6: Capacitance Characteristics**



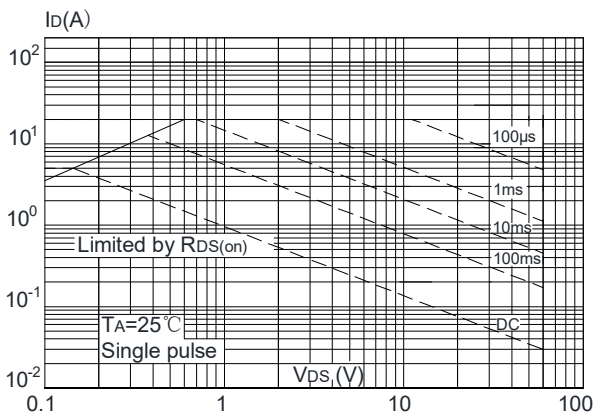
**Figure 7: Normalized Breakdown Voltage vs. Junction Temperature**



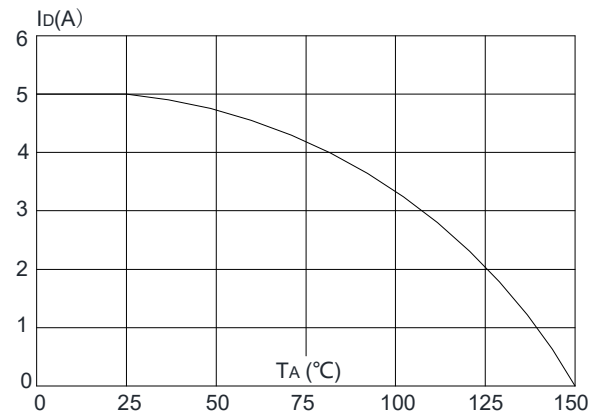
**Figure 8: Normalized on Resistance vs. Junction Temperature**



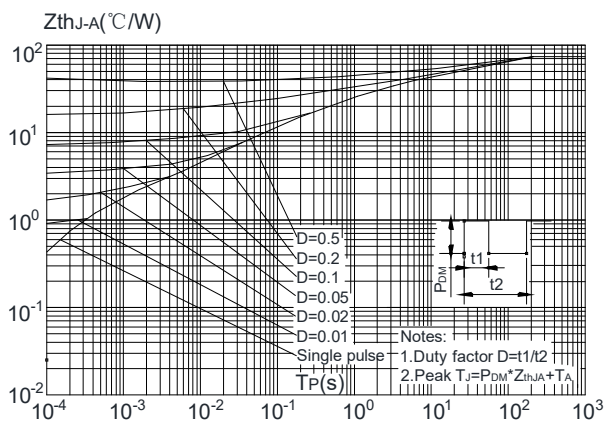
**Figure 9: Maximum Safe Operating Area**



**Figure 10: Maximum Continuous Drain Current vs. Ambient Temperature**



**Figure 11: Maximum Effective Transient Thermal Impedance, Junction-to-Ambient**



### Test Circuit

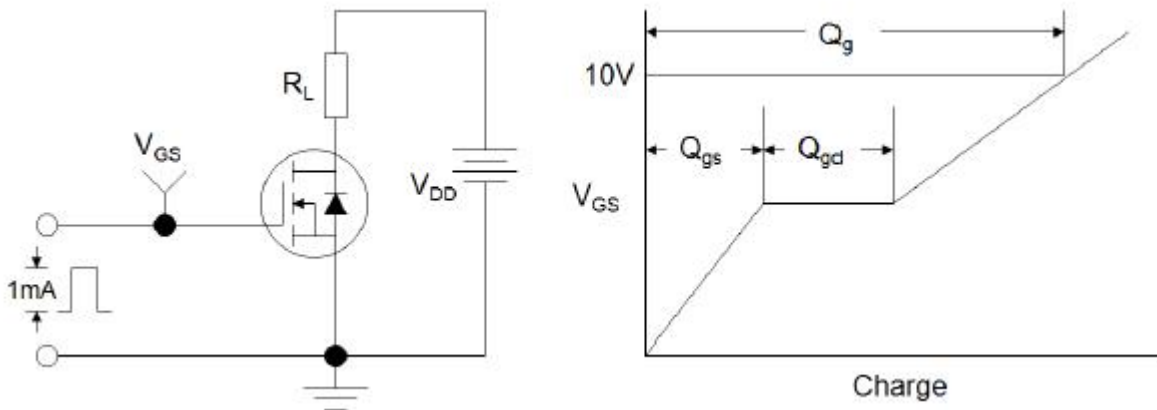


Figure1:Gate Charge Test Circuit & Waveform

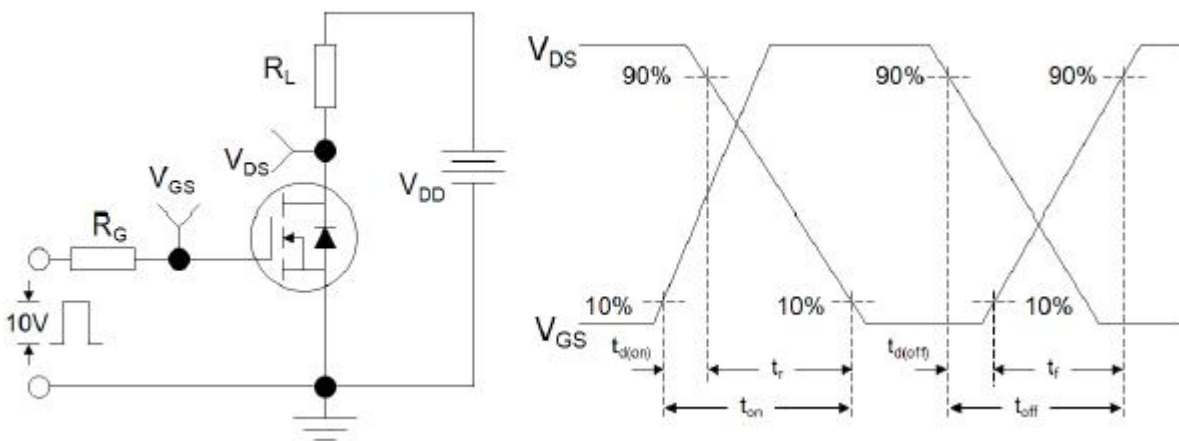


Figure 2: Resistive Switching Test Circuit & Waveforms

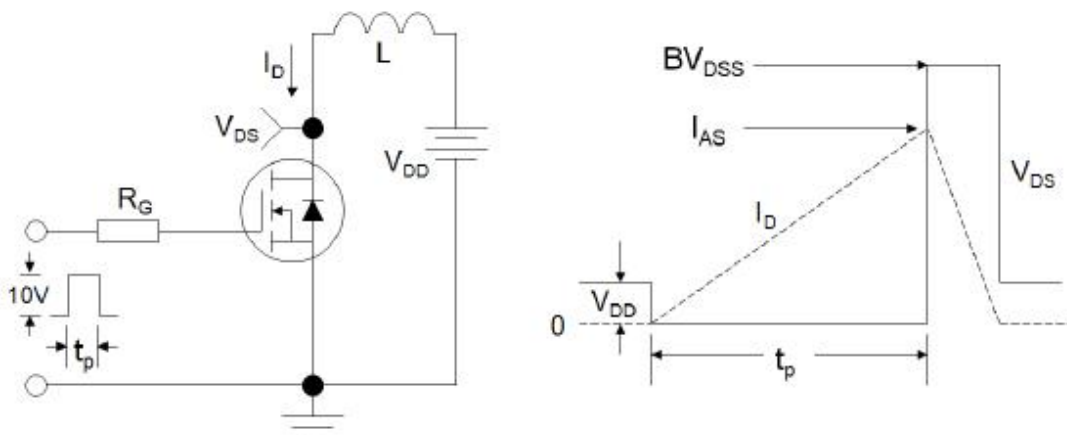


Figure 3:Unclamped Inductive Switching Test Circuit & Waveforms