

N-channel Enhancement Mode Power MOSFET

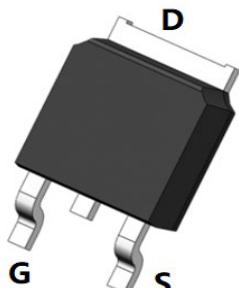
Features

- $V_{DS} = 150V$, $I_D = 40 A$
- $R_{DS(ON)} < 45 m\Omega @ V_{GS} = 10V$
- $R_{DS(ON)} < 50 m\Omega @ V_{GS} = 4.5V$

General Features

- Advanced Trench Technology
- Provide Excellent RDS(ON) and Low Gate Charge
- Lead Free and Green Available

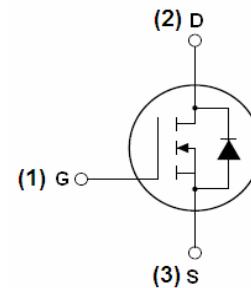
100% UIS TESTED!
100% ΔV_{ds} TESTED!



TO-252-2L Top View



Pin Assignment



Schematic Diagram

Absolute Maximum Ratings ($T_c=25^\circ C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	150	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current-Continuous	I_D	40	A
Drain Current-Continuous($T_c=100^\circ C$)	$I_D(100^\circ C)$	29	A
Pulsed Drain Current	I_{DM}	164	A
Maximum Power Dissipation	P_D	140	W
Derating factor		0.93	W/ $^\circ C$
Single pulse avalanche energy ^(Note 5)	E_{AS}	310	mJ
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 175	$^\circ C$

Thermal Characteristic

Thermal Resistance, Junction-to-Case ^(Note 2)	$R_{\theta JC}$	1.07	$^\circ C/W$
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Electrical Characteristics ($T_c=25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{\text{GS}}=0\text{V}, I_{\text{D}}=250\mu\text{A}$	150	170	-	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{\text{DS}}=150\text{V}, V_{\text{GS}}=0\text{V}$	-	-	1	μA
Gate-Body Leakage Current	I_{GSS}	$V_{\text{GS}}=\pm20\text{V}, V_{\text{DS}}=0\text{V}$	-	-	±100	nA
On Characteristics <small>(Note 3)</small>						
Gate Threshold Voltage	$V_{\text{GS(th)}}$	$V_{\text{DS}}=V_{\text{GS}}, I_{\text{D}}=250\mu\text{A}$	2.5	4.5		V
Drain-Source On-State Resistance	$R_{\text{DS(ON)}}$	$V_{\text{GS}}=10\text{V}, I_{\text{D}}=18\text{A}$	-	45		$\text{m}\Omega$
Forward Transconductance	g_{FS}	$V_{\text{DS}}=15\text{V}, I_{\text{D}}=18\text{A}$	38	-	-	S
Dynamic Characteristics <small>(Note 4)</small>						
Input Capacitance	C_{iss}	$V_{\text{DS}}=25\text{V}, V_{\text{GS}}=0\text{V}, F=1.0\text{MHz}$	-	4200	-	PF
Output Capacitance	C_{oss}		-	203	-	PF
Reverse Transfer Capacitance	C_{rss}		-	96	-	PF
Switching Characteristics <small>(Note 4)</small>						
Turn-on Delay Time	$t_{\text{d(on)}}$	$V_{\text{DD}}=30\text{V}, I_{\text{D}}=2\text{A}, R_{\text{L}}=15\Omega$ $V_{\text{GS}}=10\text{V}, R_{\text{G}}=2.5\Omega$	-	17.8	-	nS
Turn-on Rise Time	t_{r}		-	11.8	-	nS
Turn-Off Delay Time	$t_{\text{d(off)}}$		-	56	-	nS
Turn-Off Fall Time	t_{f}		-	14.6	-	nS
Total Gate Charge	Q_{g}	$V_{\text{DS}}=30\text{V}, I_{\text{D}}=30\text{A}, V_{\text{GS}}=10\text{V}$		105	-	nC
Gate-Source Charge	Q_{gs}			21	-	nC
Gate-Drain Charge	Q_{gd}			31.5	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage <small>(Note 3)</small>	V_{SD}	$V_{\text{GS}}=0\text{V}, I_{\text{s}}=18\text{A}$	-	0.82	1.2	V
Diode Forward Current <small>(Note 2)</small>	I_{s}		-	-	40	A
Reverse Recovery Time	t_{rr}	$T_{\text{J}} = 25^\circ\text{C}, \text{IF} = 18\text{A}$ $dI/dt = 100\text{A}/\mu\text{s}$ <small>(Note 3)</small>	-	70	-	nS
Reverse Recovery Charge	Q_{rr}		-	230	-	nC
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

Notes:

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, $t \leq 10$ sec.
3. Pulse Test: Pulse Width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$.
4. Guaranteed by design, not subject to production
5. EAS condition: $T_j=25^\circ\text{C}, V_{\text{DD}}=50\text{V}, V_{\text{G}}=10\text{V}, L=0.5\text{mH}, R_g=25\Omega$

Typical Electrical and Thermal Characteristics (Curves)

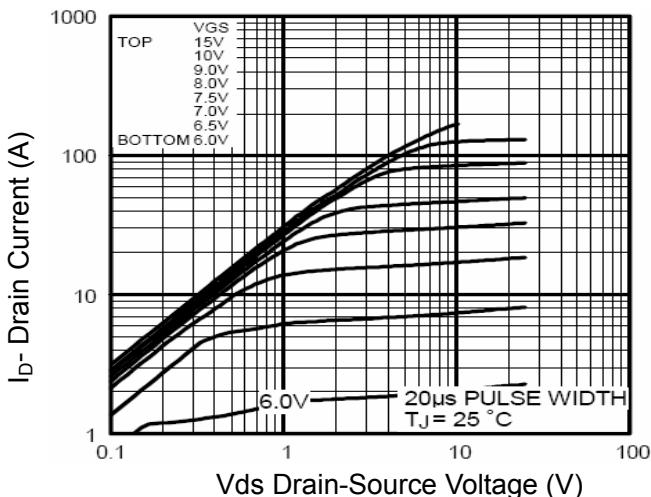


Figure 1 Output Characteristics

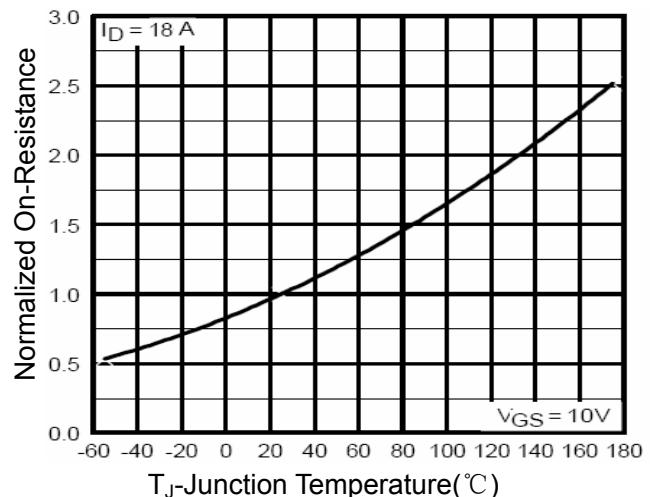


Figure 4 Rdson-JunctionTemperature

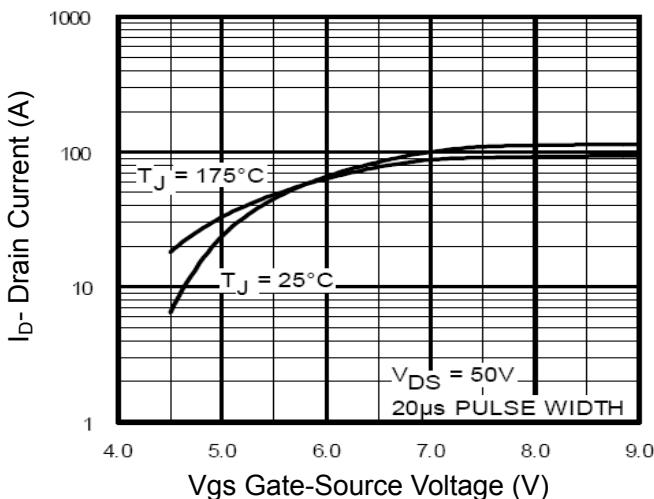


Figure 2 Transfer Characteristics

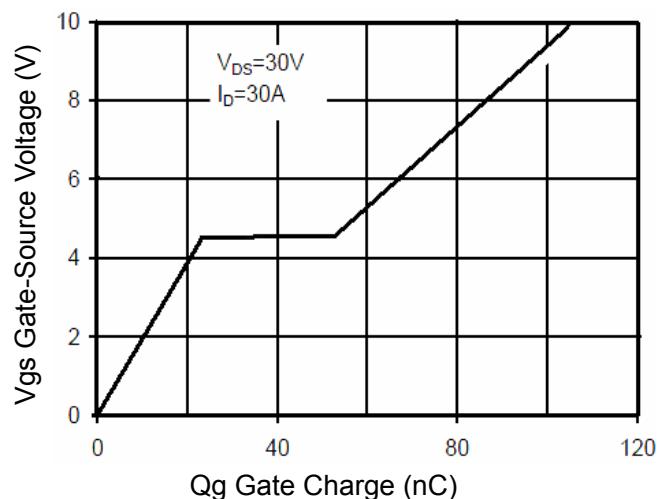


Figure 5 Gate Charge

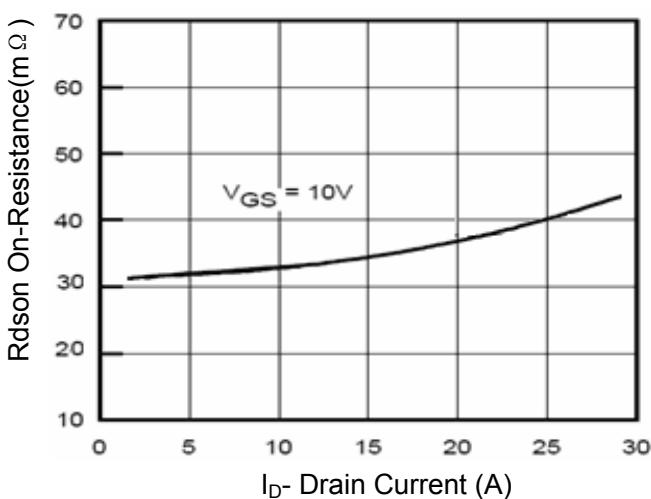


Figure 3 Rdson- Drain Current

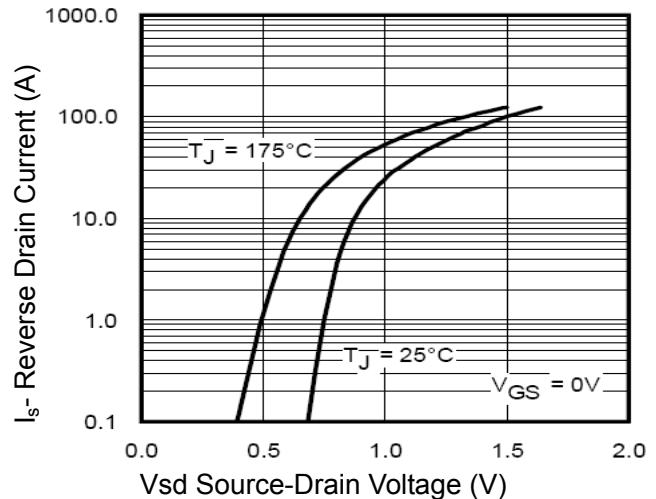
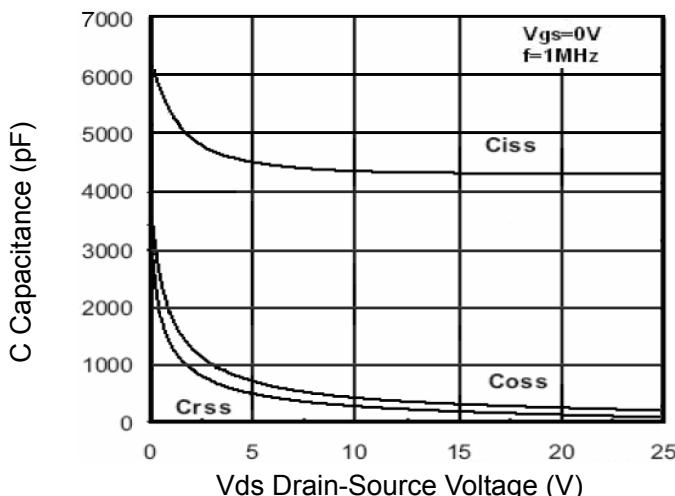
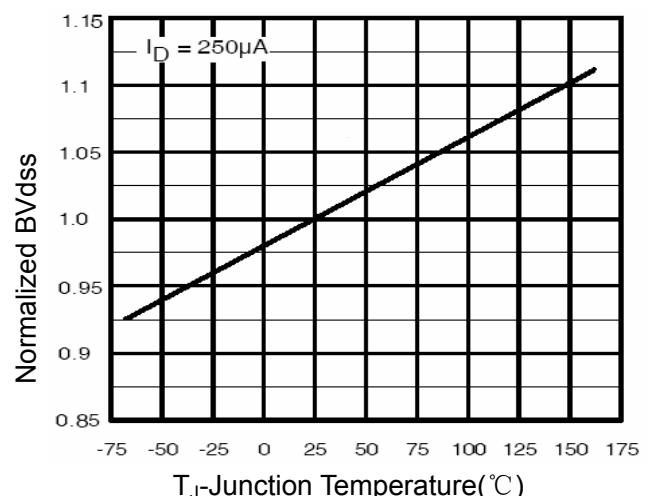
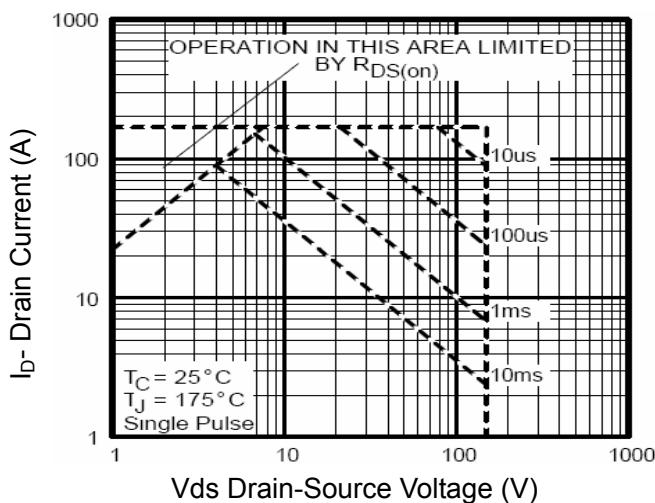
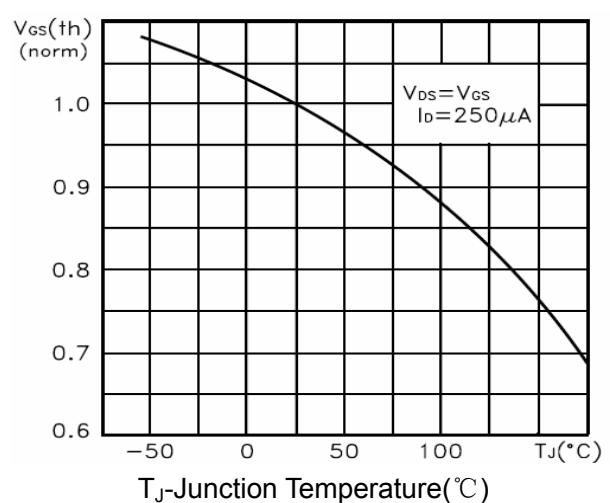
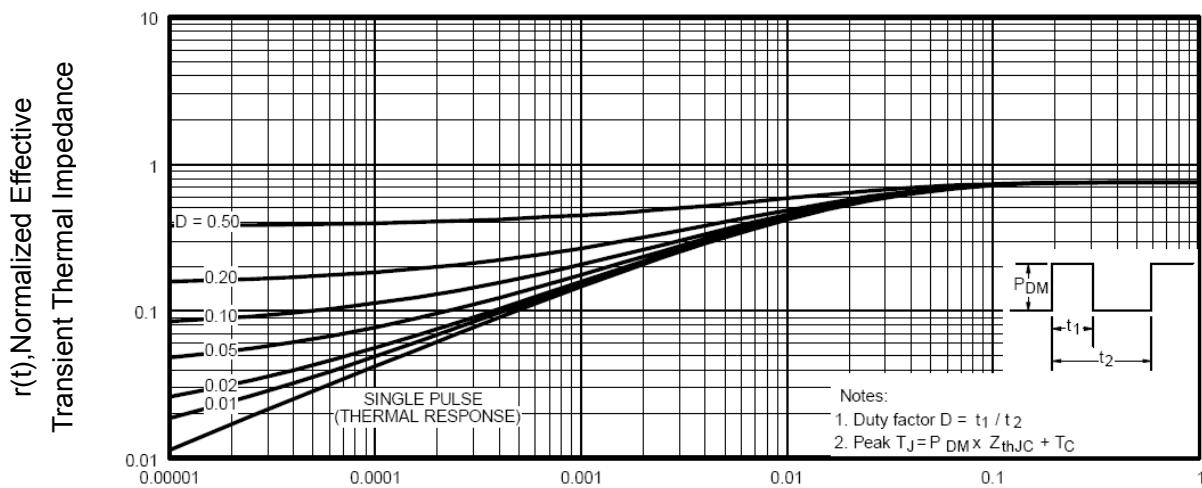


Figure 6 Source- Drain Diode Forward


Figure 7 Capacitance vs Vds

Figure 9 BV_{dss} vs Junction Temperature

Figure 8 Safe Operation Area

Figure 10 $V_{GS(th)}$ vs Junction Temperature

Figure 11 Normalized Maximum Transient Thermal Impedance