

P-channel Enhancement Mode Power MOSFET

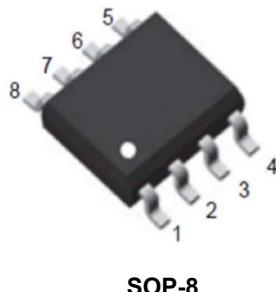
Features

- $V_{DS} = -30V$, $I_D = -9A$
- $R_{DS(ON)} < 16 \text{ m}\Omega @ V_{GS} = -10V$
- $R_{DS(ON)} < 23 \text{ m}\Omega @ V_{GS} = -4.5V$

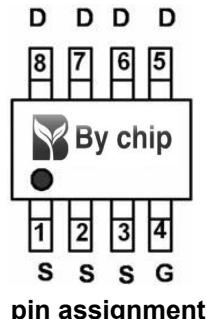
General Features

- Advanced Trench Technology
- Provide Excellent $R_{DS(ON)}$ and Low Gate Charge
- Lead Free and Green Available

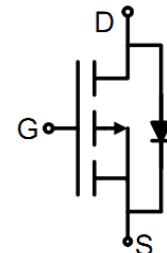
100% UIS TESTED!
100% ΔV_{ds} TESTED!



SOP-8



pin assignment



Schematic diagram

Absolute Maximum Ratings $T_C = 25^\circ\text{C}$, unless otherwise noted

Parameter	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	-30	V
Continuous Drain Current	I_D	-9	A
Pulsed Drain Current (note1)	I_{DM}	-36	A
Gate-Source Voltage	V_{GS}	± 20	V
Power Dissipation	P_D	2.7	W
Single Pulse Avalanche Energy (note3)	EAS	231	mJ
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 To 150	$^\circ\text{C}$

Thermal Resistance

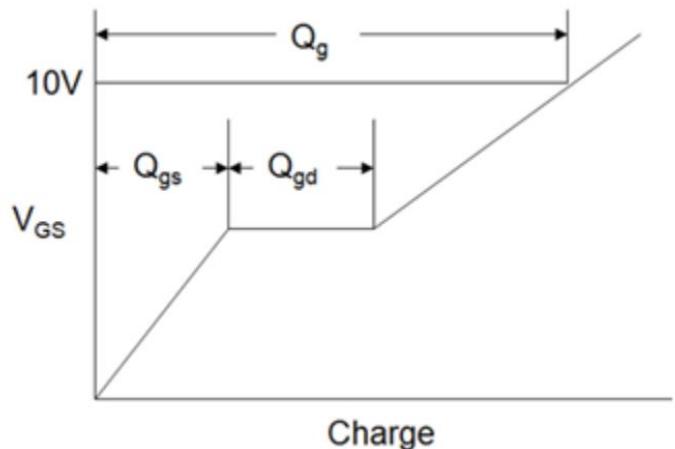
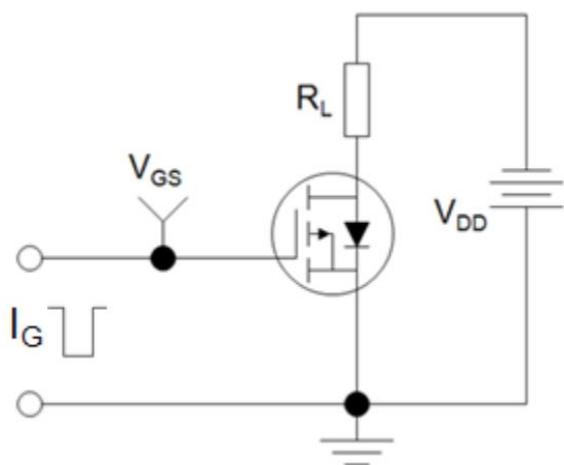
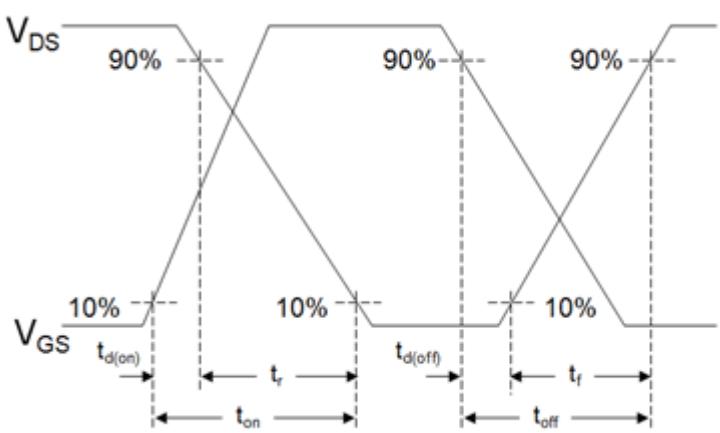
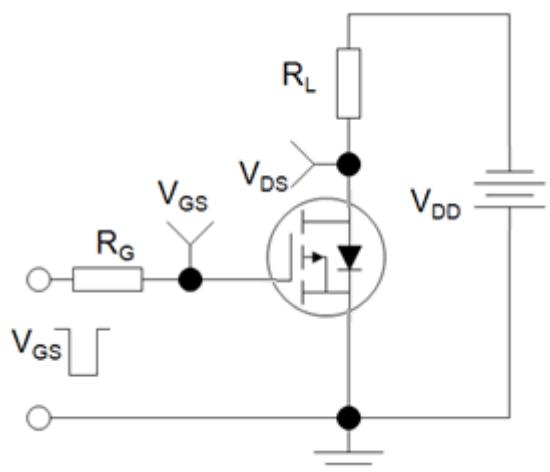
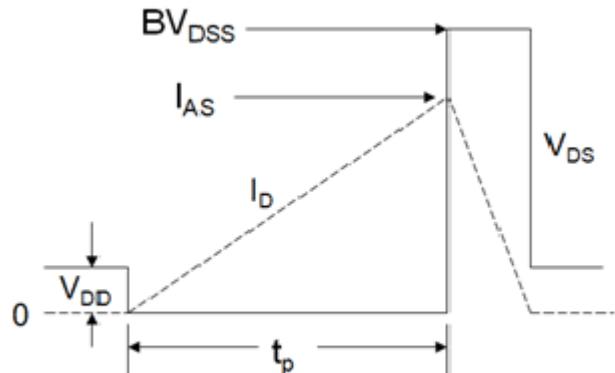
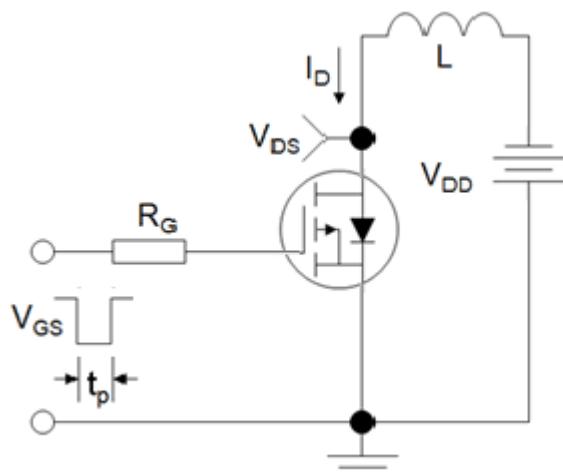
Parameter	Symbol	Value	Unit
Thermal Resistance, Junction-to-Ambient	R_{thJA}	47	$^\circ\text{C/W}$

Specifications $T_J = 25^\circ\text{C}$, unless otherwise noted

Parameter	Symbol	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
Static Parameters						
Drain-Source Breakdown Voltage	$V_{(\text{BR})\text{DSS}}$	$V_{\text{GS}} = 0\text{V}, I_D = -250\mu\text{A}$	-30	--	--	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{\text{DS}} = -30\text{V}, V_{\text{GS}} = 0\text{V}$	--	--	-1	μA
Gate-Source Leakage	I_{GSS}	$V_{\text{GS}} = \pm 20\text{V}$	--	--	± 100	nA
Gate-Source Threshold Voltage	$V_{\text{GS}(\text{th})}$	$V_{\text{DS}} = V_{\text{GS}}, I_D = -250\mu\text{A}$	-1		-3	V
Drain-Source On-Resistance	$R_{\text{DS}(\text{on})}$	$V_{\text{GS}} = -10\text{V}, I_D = -3\text{A}$	--		16	$\text{m}\Omega$
		$V_{\text{GS}} = -4.5\text{V}, I_D = -2\text{A}$	--		23	
Dynamic Parameters						
Input Capacitance	C_{iss}	$V_{\text{GS}} = 0\text{V}, V_{\text{DS}} = -15\text{V}, f = 1.0\text{MHz}$	--	1253	--	pF
Output Capacitance	C_{oss}		--	181	--	
Reverse Transfer Capacitance	C_{rss}		--	158	--	
Total Gate Charge	Q_g	$V_{\text{DD}} = -15\text{V}, I_D = -3\text{A}, V_{\text{GS}} = -10\text{V}$	--	24.5	--	nC
Gate-Source Charge	Q_{gs}		--	3	--	
Gate-Drain Charge	Q_{gd}		--	6	--	
Turn-on Delay Time	$t_{\text{d}(\text{on})}$	$V_{\text{DD}} = -15\text{V}, I_D = -3\text{A}, R_G = 1\Omega$	--	8	--	ns
Turn-on Rise Time	t_r		--	9	--	
Turn-off Delay Time	$t_{\text{d}(\text{off})}$		--	26	--	
Turn-off Fall Time	t_f		--	8	--	
Drain-Source Body Diode Characteristics						
Continuous Body Diode Current	I_S	$T_C = 25^\circ\text{C}$	--	--	-9	A
Body Diode Voltage	V_{SD}	$T_J = 25^\circ\text{C}, I_{\text{SD}} = -3\text{A}, V_{\text{GS}} = 0\text{V}$	--	--	-1.2	V

Notes

1. Repetitive Rating: Pulse width limited by maximum junction temperature
2. Identical low side and high side switch with identical R_G
3. $V_{\text{DD}} = -30\text{V}, R_G = 25\Omega, L=0.5\text{ mH}$, Starting $T_J = 25^\circ\text{C}$.

Gate Charge Test Circuit**Switch Time Test Circuit****EAS Test Circuit**

Typical Characteristics $T_J = 25^\circ\text{C}$, unless otherwise noted

Figure 1. Output Characteristics

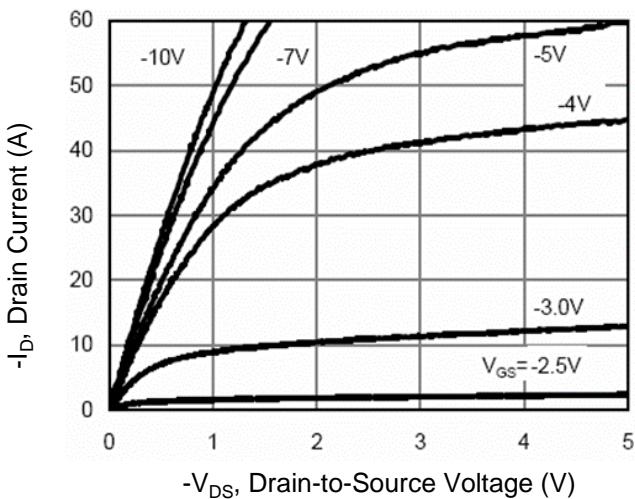


Figure 2. Transfer Characteristics

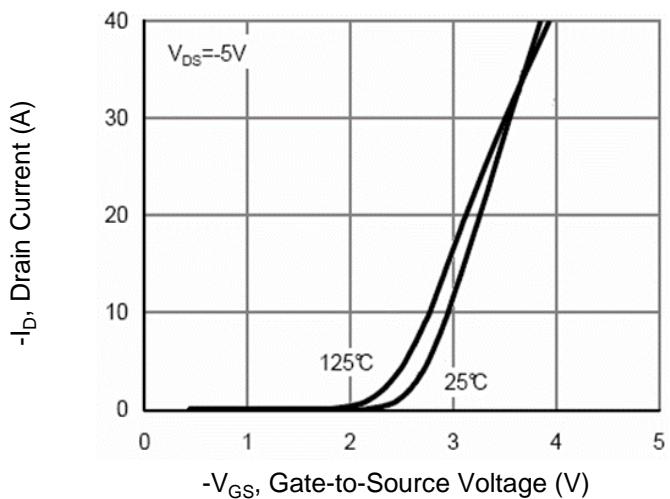


Figure 3. R_{DSON} vs V_{GS}

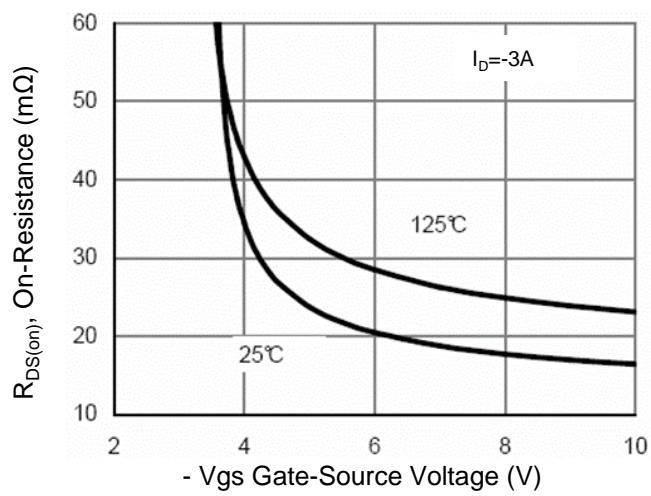


Figure 4. Gate Charge

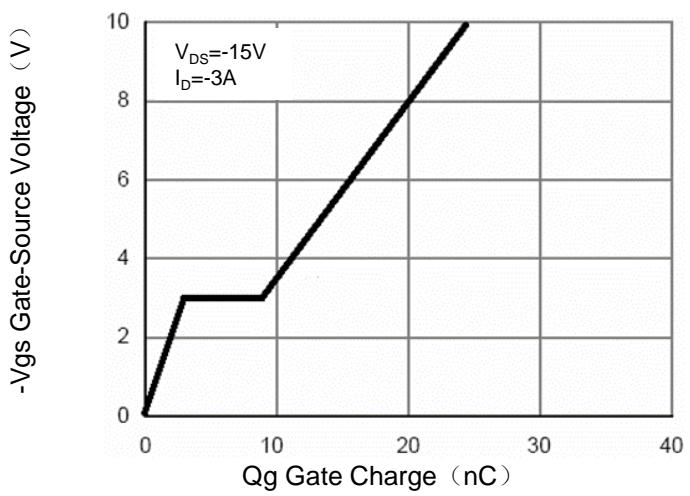


Figure 5. Capacitance vs Vds

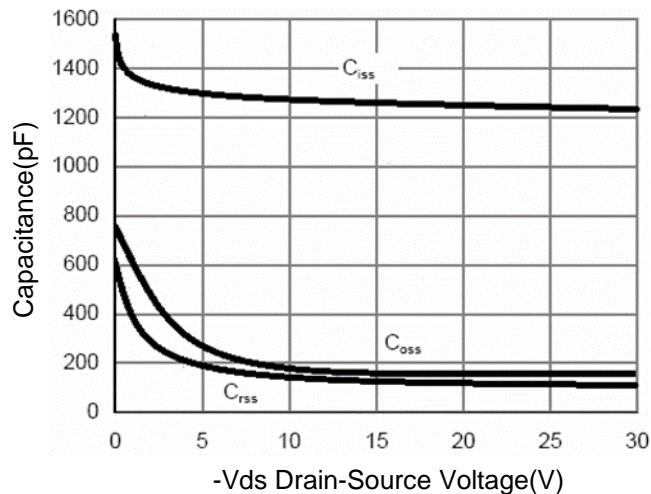
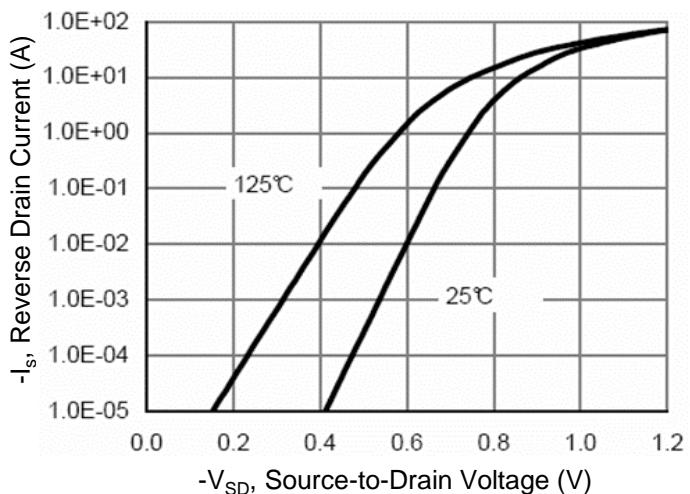


Figure 6. Source-Drain Diode Forward



Typical Characteristics $T_J = 25^\circ\text{C}$, unless otherwise noted

Figure 7. Drain-Source On-Resistance

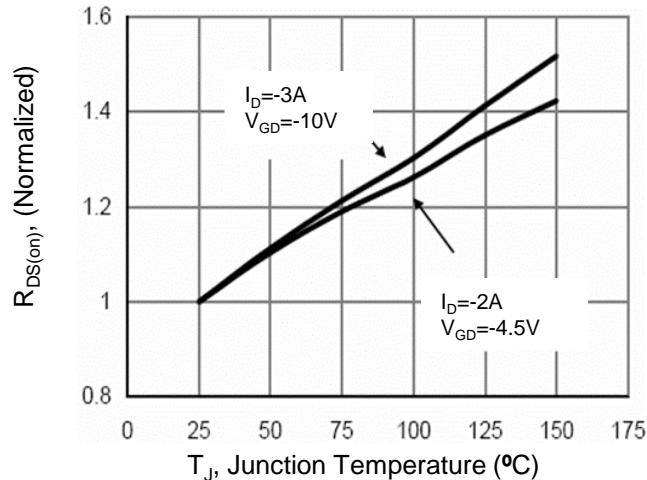


Figure 10. Safe Operation Area

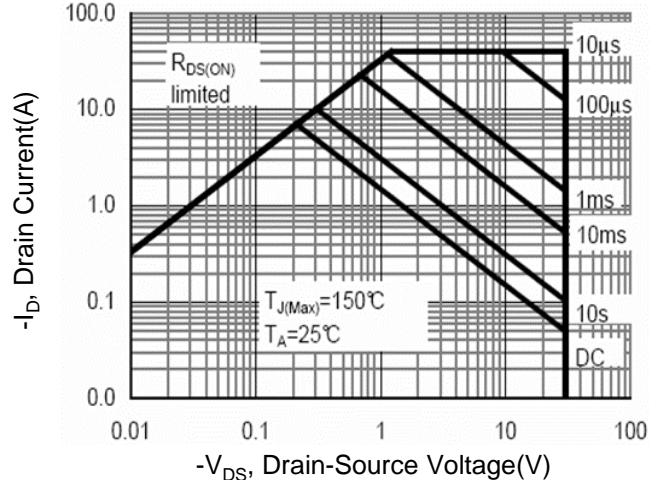


Figure 9. Normalized Maximum Transient Thermal Impedance

