

P-channel Enhancement Mode Power MOSFET

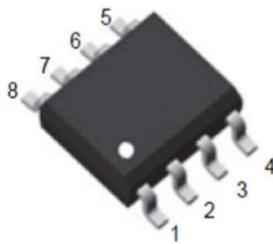
Features

- $V_{DS} = -60V$, $I_D = -7A$
 $R_{DS(ON)} < 55m\Omega$ @ $V_{GS} = -10V$
 $R_{DS(ON)} < 65m\Omega$ @ $V_{GS} = -4.5V$

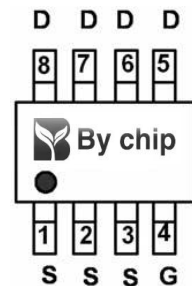
General Features

- Advanced Trench Technology
- Provide Excellent $R_{DS(ON)}$ and Low Gate Charge
- Lead Free and Green Available

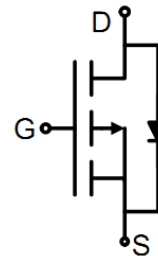
100% UIS TESTED!
 100% ΔV_{ds} TESTED!



SOP-8



pin assignment



Schematic diagram

Absolute Maximum Ratings ($T_C = 25^\circ C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	-60	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current-Continuous	I_D	-7	A
Pulsed Drain Current	I_{DM}	-30	A
Maximum Power Dissipation	P_D	3.0	W
Single pulse avalanche energy ^(Note 5)	E_{AS}	65	mJ
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 150	$^\circ C$

Thermal Characteristic

Thermal Resistance, Junction-to-Ambient ^(Note 2)	$R_{\theta JC}$	41.7	$^\circ C/W$
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Electrical Characteristics ($T_C=25^{\circ}\text{C}$ unless otherwise noted)

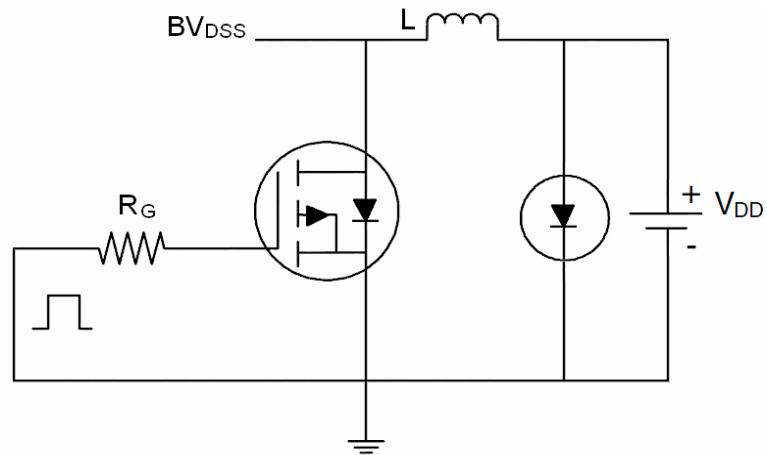
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=-250\mu A$	-60	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=-60V, V_{GS}=0V$	-	-	-1	μA
Gate-Body Leakage Current	I_{GSS}	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	± 100	nA
On Characteristics (Note 3)						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=-250\mu A$	-1.0		-3.0	V
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS}=-10V, I_D=-7A$	-		55	m Ω
		$V_{GS}=-4.5V, I_D=-7A$	-		65	m Ω
Forward Transconductance	g_{FS}	$V_{DS}=-5V, I_D=-7A$	-	15	-	S
Dynamic Characteristics (Note 4)						
Input Capacitance	C_{iss}	$V_{DS}=-30V, V_{GS}=0V,$ $F=1.0\text{MHz}$	-	1108	-	PF
Output Capacitance	C_{oss}		-	73.7	-	PF
Reverse Transfer Capacitance	C_{rss}		-	58.2	-	PF
Switching Characteristics (Note 4)						
Turn-on Delay Time	$t_{d(on)}$	$V_{DD}=-30V, R_L=4.2\Omega,$ $V_{GS}=-10V, R_G=3\Omega$	-	8	-	nS
Turn-on Rise Time	t_r		-	4	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	32	-	nS
Turn-Off Fall Time	t_f		-	7	-	nS
Total Gate Charge	Q_g	$V_{DS}=-30V, I_D=-7A,$ $V_{GS}=-10V$	-	23.4	-	nC
Gate-Source Charge	Q_{gs}		-	4.1	-	nC
Gate-Drain Charge	Q_{gd}		-	4.8	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage	V_{SD}	$V_{GS}=0V, I_S=-7A$	-		-1.2	V
Diode Forward Current	I_S		-	-	-7	A
Reverse Recovery Time	t_{rr}	$T_J = 25^{\circ}\text{C}, I_F = -7A$	-	25		nS
Reverse Recovery Charge	Q_{rr}	$di/dt = -100A/\mu s$ (Note 3)	-	31		nC

Notes:

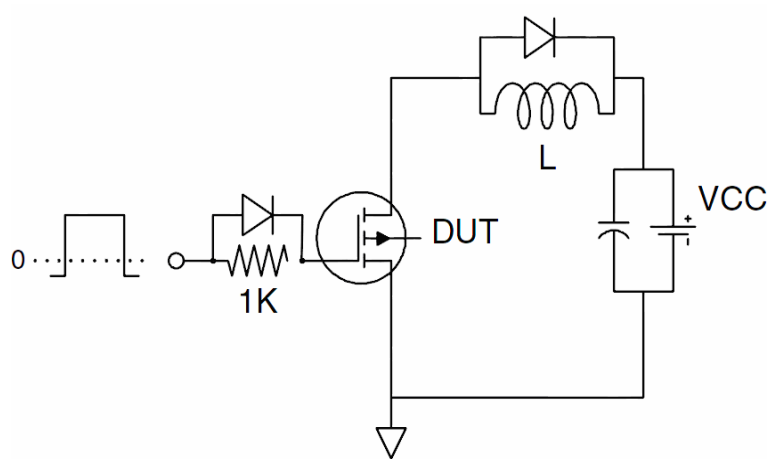
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, $t \leq 10$ sec.
3. Pulse Test: Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$.
4. Guaranteed by design, not subject to production

Test Circuit

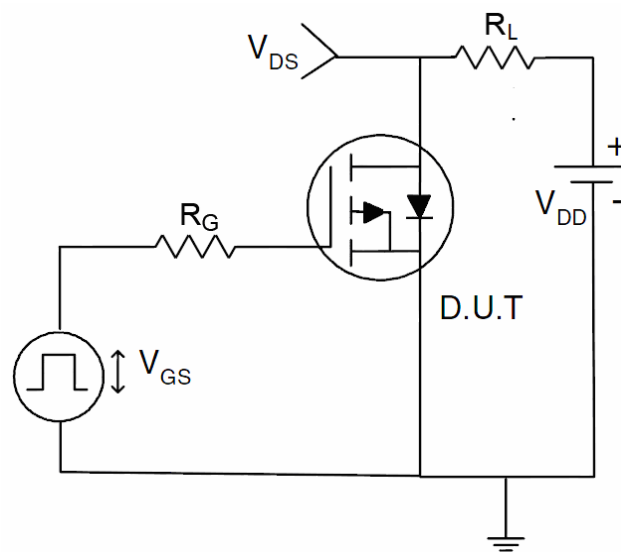
1) E_{AS} Test Circuit



2) Gate Charge Test Circuit



3) Switch Time Test Circuit



Typical Electrical and Thermal Characteristics (Curves)

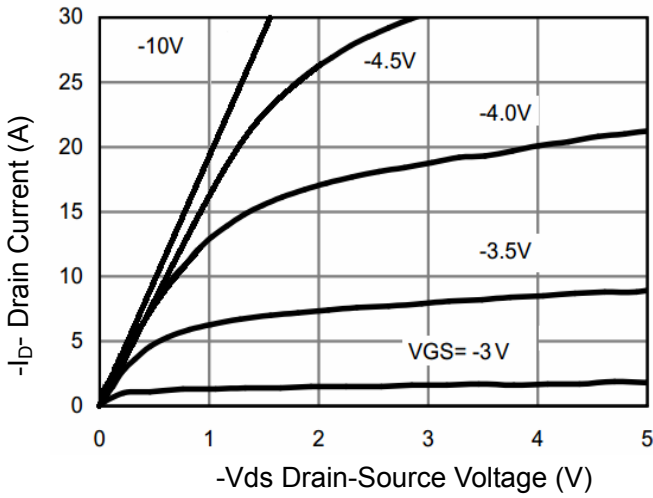


Figure 1 Output Characteristics

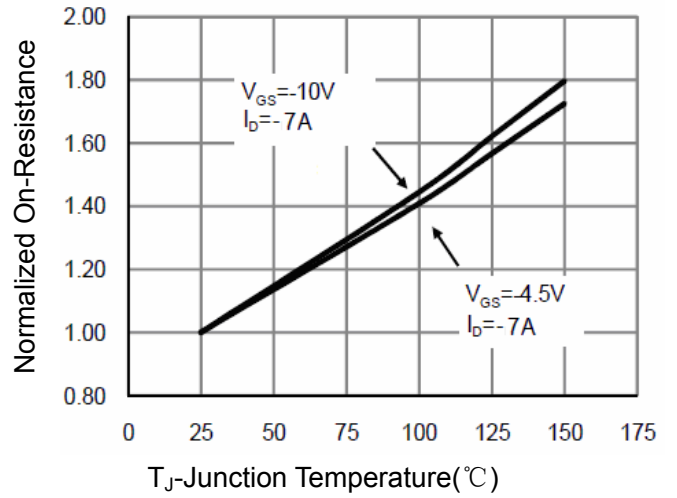


Figure 4 R_{dson} -Junction Temperature

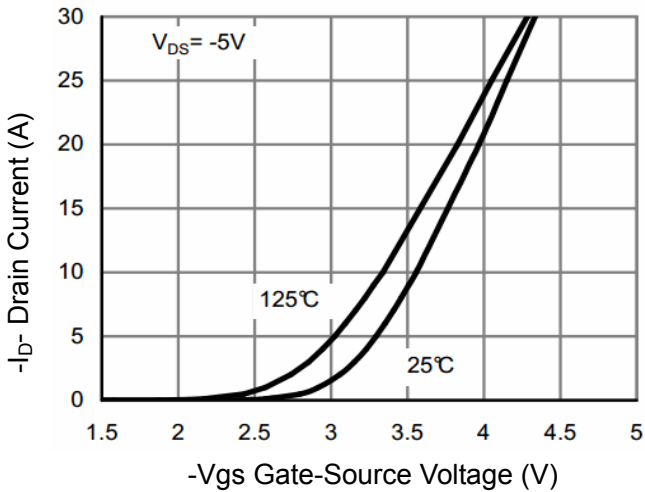


Figure 2 Transfer Characteristics

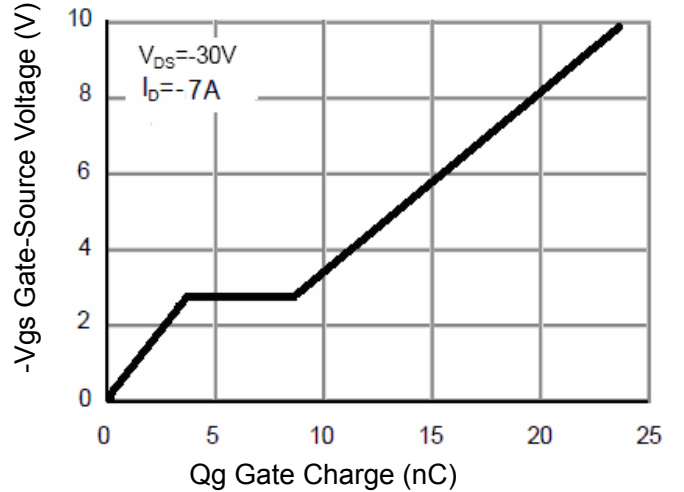


Figure 5 Gate Charge

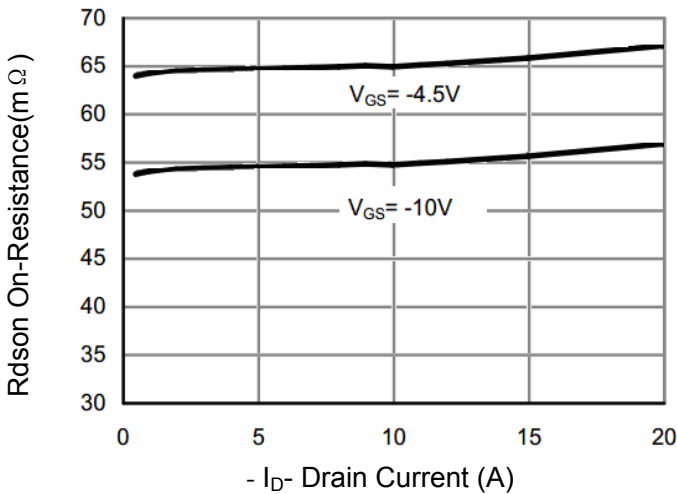


Figure 3 R_{dson} - Drain Current

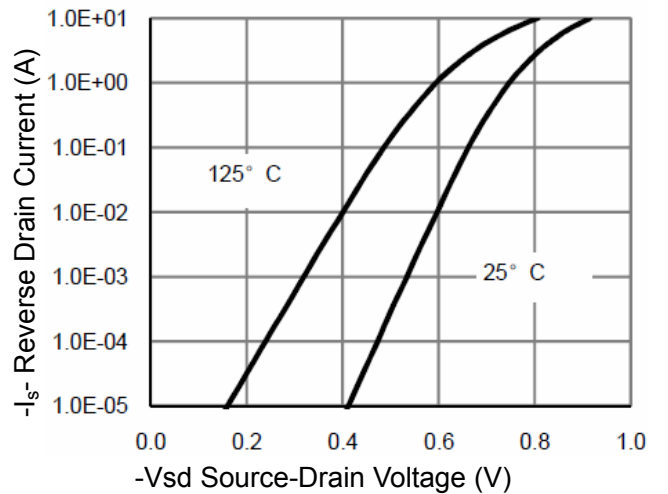


Figure 6 Source- Drain Diode Forward

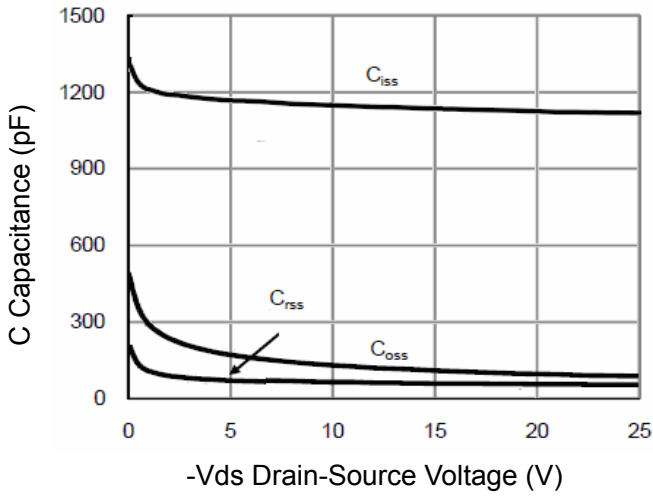


Figure 7 Capacitance vs Vds

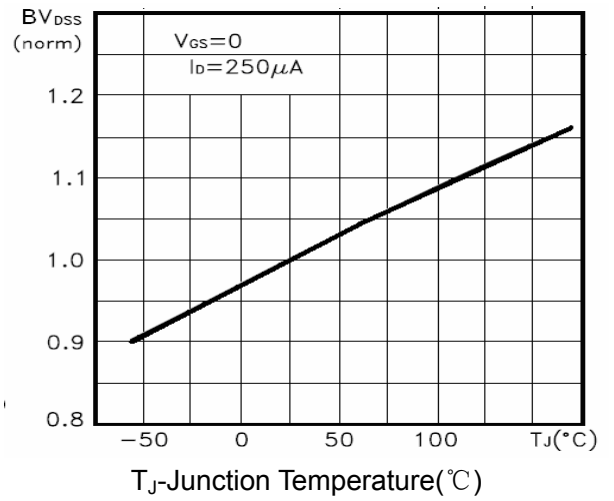


Figure 9 BV_{DSS} vs Junction Temperature

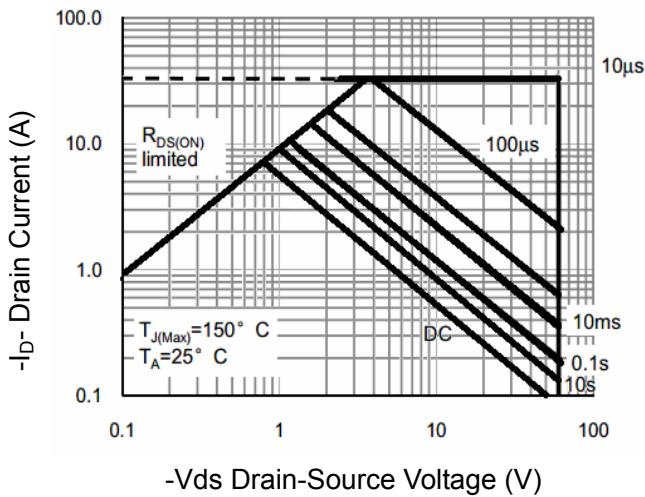


Figure 8 Safe Operation Area

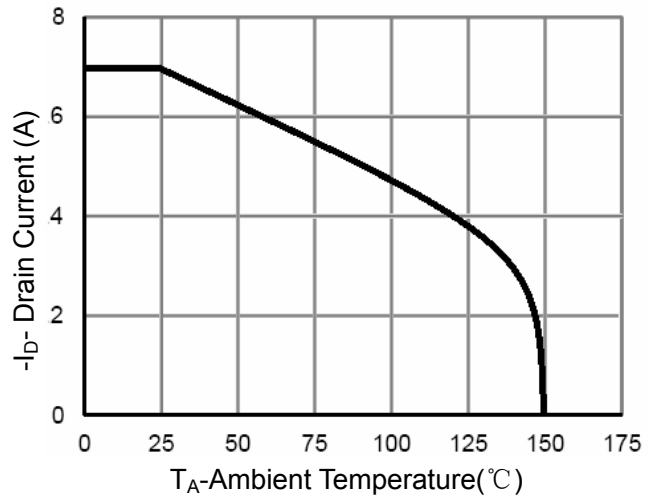


Figure 10 I_D Current De-rating

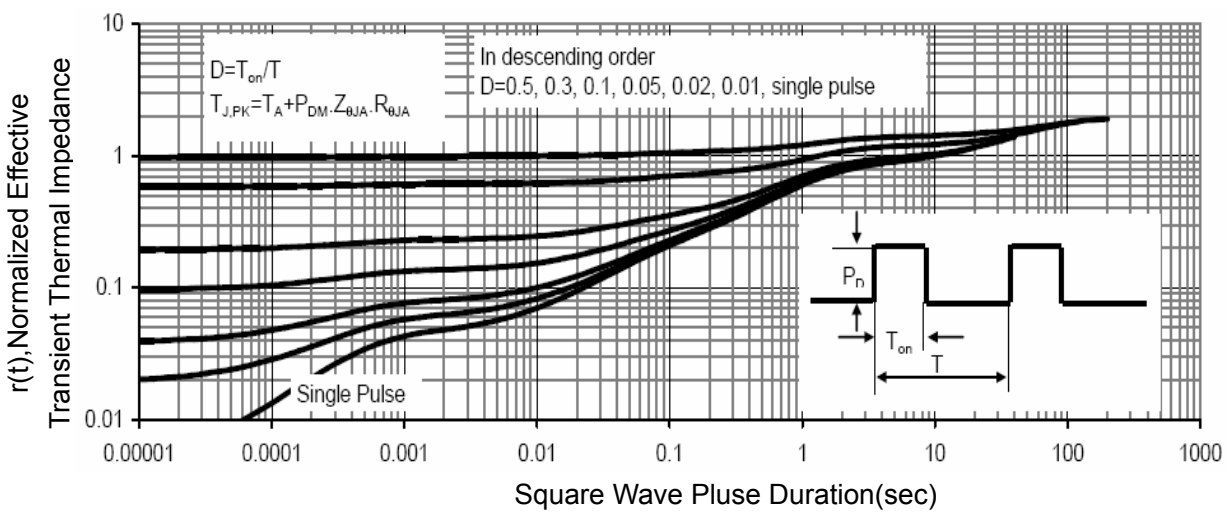


Figure 11 Normalized Maximum Transient Thermal Impedance